Test Org.*	Device	Function	Technology	Mfr.	Effective SEU LET* Threshold	Device Xsection (cm^2)	Bits Tested	Bit Xsection (cm^2)	Test Date	LUth	LU Xsection (cm^2)	Fac.	Remarks 31-Aug-99
		DRAMs											
	Note: Entries in **RED** indicate data added since the 1997 Compendium.												
NRL	4164	64K x 1	NMOS	INT									
IBM	44400	1M x 4	CMOS	TIX					1990		2.0E-06		
ESA	44400	1M x 4	CMOS Rev B design (shrink)	TIX	1.5	2.0E+00		5.0E-07		>165			TIX in Japan
GSFC	**0116400J1C-70 rev C**	**4M x 4**	**CMOS**	**IBM**	**3**	**7.0E-02**			**Dec-96**	**50**	**2.0E-04**	**UCD**	**LaBel, et al, 96IEEE Wrkshp Rec., pg 19. Cell errors.**
GSFC	**0116400J1C-70 rev C**	**4M x 4**	**CMOS**	**IBM**	**5**	**7.0E-02**			**Dec-96**	**50**	**2.0E-04**	**UCD**	**LaBel, et al, 96IEEE Wrkshp Rec., pg 19. Block errors.**
GSFC	**0116400J1D**	**4M x 4**	**CMOS**	**IBM**	**<3.38**				**1996**	**>11.5**		**UCB TAM**	**LaBel, et al, 97IEEE Wrkshp Rec., pg 14. Bit errors.**
GSFC	**0116400J1D**	**4M x 4**	**CMOS**	**IBM**	**3.9**				**1996**	**>11.5**		**UCB TAM**	**LaBel, et al, 97IEEE Wrkshp Rec., pg 14. Bit and block errors.**
ESA	**0117400BT1F-60**	**4M x 4 (3.3 V)**	**CMOS (IBM - ES4)**	**IBM**	**~1**			**4.0E-08**	**1997**			**CYC**	**Harboe-Sorensen, et al, 98IEEE Wrkshp Rec., pg 74.**
CNES	01G9274		CMOS	IBM	2.5			2.4	1993				D/C ES.
SEI	**14C0164RP**	**4M x 4**	**CMOS**	**HTC**	**4.5**	**3.0E-01**			**Jan-97**	**>89**		**UCD TAM**	**Layton, et al, 98IEEE Wrkshp Rec., pg 170.**
ARSP	2164A	64K x 1	NMOS	INT	~1	2.0E-01		300	Dec-89				
ESA	44100DM-80	16K x 1	CMOS(EPIC) 0.75 µm line width	TIX	1.5	2.0E+00		50	1993	>165			
ESA	D424100V-80	4M x 1	CMOS	NEC	~1			0	1991	>50			
JPL	**D426S165G5**	**4M x 16 EDO (3.3 V)**	**CMOS**	**NEC**	**~1**			**1.0E-07**	**1998**			**BNL**	**Swift, RADECS98 preprint. D/C 9738KE006**
ROCK	EDI 41024C100QB	1M x 1		EDI	1.4	1.1E-01		10	Apr-92	>82			
ESA	**HM51W16100B**	**CMOS**	**CMOS**	**HTC**	**~1**			**8**	**1997**			**CYC**	**Harboe-Sorensen, et al, 98IEEE Wrkshp Rec., pg 74.**
ESA	HM514100ZP8	4M x 1	CMOS	HTC	~2			12	Sep-91	>40			
JPL	**HM5165165AJ**	**4M x 16 EDO**	**CMOS**	**HTC**	**<20**			**1.0E-06**	**1998**			**BNL**	**Swift, RADECS98 preprint. D/C 9737**
ESA	**HM51W16100B**	**CMOS**	**CMOS**	**HTC**	**~1**			**8**	**1997**			**CYC**	**Harboe-Sorensen, et al, 98IEEE Wrkshp Rec., pg 74.**
ESA	HYB514100J-10	4M x 1	CMOS (n-well)	SIE	~1			6.0E-07	Sep-91	>40			
JPL	IS256		NMOS	MCN	1	6.0E-01		2.4E-06	Aug-87		1.0E-04		
JPL	IS256 (with EDAC)		NMOS	MCN	<2	1.0E-02			Aug-87				
ESA	KM41C16000J	16M x 1	CMOS	SAM	<1			2.0E-07	1995	>110			
ESA	KM41C4000Z-8	4M x 1	CMOS	SAM	~2			4.0E-07	Sep-91	>40			
GSFC	KM44C4000AJ-7	4M x 1	CMOS	SAM	<1.46	3.0E+00		1.7E-07	Jul-94	>110			
ICI	**KM44S16030CT-GL**	**16M x 4 (3.3 V)**	**CMOS**	**SAM**	**~20**	**~2.5E+01**			**1998**	**>50**			**Henson, et al, 99IEEE Wrkshp Rec. Preprint (paper W-7). Static mode. Multiple upsets and stuck bits seen at high LETs.**
ICI	**KM44S16030CT-GL**	**16M x 4 (3.3 V)**	**CMOS**	**SAM**	**~20**	**~1.0E+01**			**1998**	**>50**			**Henson, et al, 99IEEE Wrkshp Rec. Preprint (paper W-7). Dynamic mode. Multiple upsets and stuck bits seen at high LETs.**

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Test Org.*	Device	Function	Technology	Mfr.	Effective SEU LET* Threshold	Device Xsection (cm^2)	Bits Tested	Bit Xsection (cm^2)	Test Date	LUth	LU Xsection (cm^2)	Fac.	Remarks 31-Aug-99
ICI	**KM44S32030CT-GL**	**32M x 4 (3.3 V)**	**CMOS**	**SAM**	**~15**	**~4.0E+01**			**1998**	**>82**			**Henson, et al, 99IEEE Wrkshp Rec. Preprint (paper W-7). Dynamic and static modes.**
ESA	KM44C4000J-6	4M x 1	CMOS	SAM	<1			2.0E-07	1995	>110			
ESA	**KM44V4100AJ**	**4M x 4 (3.3 V)**	**CMOS**	**SAM**	**~1**			**5.0E-08**	**1997**			**CYC**	**Harboe-Sorensen, et al, 98IEEE Wrkshp Rec., pg 74.**
JPL	KM48V8004AK-6	DRAM	CMOS	SAM					Mar-97	56±4	1.3E-06		
JPL	**KM48V8104AS-6**	**8M x 8 EDO**	**CMOS**	**SAM**	**~1**			**2.0E-08**					
CNES/ALC	LUNA-C	4M x 4	CMOS/epi with ECC-- off or on	IBM	~3	~2.0E-01			1994	>120			
CNES/ALC	LUNA-C	4M x 4	CMOS/epi with ECC-- off or on	IBM	~3	3.0E-03			1994	>120			
JPL/LFS	LUNA-C DD3	4M x 4	CMOS/epi with ECC-- off	IBM	4			2.0E-08	Aug-94	>120			
CNES/ALC	LUNA-E	4M x 4	CMOS/epi without ECC	IBM	~3	1.0E-01			1994	>120			
GSFC	LUNA-ES2	4M x 4	CMOS/epi without ECC	IBM	<3.4				Mar-97	11.5	1.0E-04		
JPL	M41256	256K x 1	NMOS	ATT	<2	5.0E-01		2.0E-06					
ARSP	M5M44100	4M x 1	CMOS	MIT	<3.3	1.0E+00			Dec-94	>60			
JPL	M5M467800AJ	64M	CMOS	MIT					Mar-97	~82	1.2E-06	BNL	LU X-section still unsaturated @ LET = 82. Parts were only partially operational.
ESA	MB8116100-60PJ "F"	16M x 1	CMOS	FUJ	<1			1.0E-07 - 2.0E-07	1995	>110		BNL	Harboe-Sorensen, et al, 95IEEE Wrkshp Rec., pg 42. Row errors noted. Comparison testing done at UCL (Belgium)
GSFC	MB8116400-60PJ	16M x 1	CMOS	FUJ	<1.4	3.5E+00			May-94	>80		BNL	SEFI @ LET ~50. LaBel test
GSFC	MB8116400-60PJ	DRAM	CMOS	FUJ	<1.4	3.0E+00			Dec-96	80		BNL	LaBel, et al, 96IEEE TNS, No. 6, pg 2974. SEFI @ LET = 50. D/C 9337. Vcc = 5V.
JPL/ARSP	MB81256	256K x 1	NMOS	FUJ	~2	1.0E-01		4.0E-07				BNL	
ESA	MB814100-10PSZ	4M x 1	CMOS	FUJ	~1			8.0E-07	Sep-91	>50		IPN	RADECS 91
ROCK	MCM6605A	4K	NMOS	MOT	~14	2.0E-02		5.0E-06				UCB	
ROCK	MDM11000TMB	1M x 1	CMOS	NEC	<0.5	2.4E-01		2.4E-07	Apr-92	25	1.0E-04	BNL	Dynamic test - MOSAID MS2200 Memory tester. Fabbed at Mosaic.
ROCK	MDM14000G	4M x 1	CMOS	HTC	1.7	1.2E-01		3.0E-08	Apr-92	>82		BNL	MOSAID MS2200 Memory tester. Fabbed at Mosaic.
JPL	MDM14000GMB-80	4M x 1	CMOS-- MIT M5M44100 die	MIT					Nov-95	>87		TAM	Mosaic package. No observed stuck bits.
ESA	MKB4116	16K x 1	NMOS	MOS					Dec-91				C. S. Dyer, J. Stephen refer to calc'd SEU rate in 91IEEE TNS, No. 6, pg 1700.
JPL	MT1259	256K x 1	NMOS	MCN	<1				Dec-89			BNL	Upsets depend on bias. See 88IEEE TNS, No. 6, pg. 1644 & 89IEEE TNS, No. 6, pg. 2267.
CNES	MT4C1004C	4M x 1	CMOS/epi (0.8 µm. line width)	MCN					Jan-92	>54		IPN	Ecoffet, CNES report RA/DP/QA/CE/92-513 on Test Campaigns 8&9. D/C 9109.
ESA	MT4C1004C	4M x 1	CMOS (0.8 µm. line width)	MCN	~1.5			3.0E-07 - 8.0E-07	1991	>120		BNL & IPN	Harboe-Sorensen, RADECS 91, & 93, pg 490. D/C 2C9236C.
ARSP	MT4C4001	1M x 4	CMOS/epi (7 µm)	MCN	~3	2.0E+00			Mar-92	>100		UCB	At 70 deg. C. LU_{th} >100 at R.T.
CNES	MT4C4001	1M x 4	CMOS/epi	MCN	<0.4 to <1.7	1.0E+00		5.0E-07 - 1.5E-06	1993			IPN	Duzellier, et al, 95IEEE TNS, No. 6, pg 1797. D/C 9109 & 9248. High vs medium energy beam study. Comparison studies done at Saturne (France).

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Test Org.*	Device	Function	Technology	Mfr.	Effective SEU LET* Threshold	Device Xsection (cm^2)	Bits Tested	Bit Xsection (cm^2)	Test Date	LUth	LU Xsection (cm^2)	Fac.	Remarks 31-Aug-99
ESA	MT4C4001JC	1M x 4	engr sample-shrunk 0.6µm	lMCN	~1.5			4.0E-07 - 8.0E-07	1993	>120		IPN	Harboe-Sorensen, RADECS 93, pg 490. D/C 9244. Process D15B.
GSFC	MT4C4M4B1DW	4M x 4	CMOS	MCN	<1.4				May-94	12 to 26		BNL	LaBel. LU obscures LET_{th}.
ESA	MT4C4M4B1DW	4M x 4	CMOS	MCN	<1			1.0E-07	1995	53		BNL	Harboe-Sorensen, et al, 95IEEE Wrkshp Rec.,pg 42. Row errors =2E-4 cm2. D/C 9406B.
GSFC	MT4C4M4B1DW	DRAM	CMOS	MCN	<1.4	2.0E-01			Dec-96	12 to 26	2.0E-04	BNL	LaBel, et al, 96IEEE TNS, No. 6, pg 2974. D/C 9404. Vcc=5V.
ESA	**MT4LC4M4D42 Rev T**	**4M x 4 (3.3 V)**	**CMOS**	**MCN**	**~1**			**6.0E-08**	**1997**			**CYC**	**Harboe-Sorensen, et al, 98IEEE Wrkshp Rec., pg 74.**
IBM	SMJ27C128-25	16K x 8	CMOS	TIX					May-93			BNL	The data here was taken as a subset of the TIX SM320E15 DSP.
IBM	SMJ416400-1 thru-6	4K x 4	CMOS epi?	TIX	0.4			1.1E-08	Jan-93	>70		BNL	Functional interrupt LET(th) = 12; 2.7E-06 cm^2. WP-2 (Jim Pollack)
CERT/ CNES	SMJ416400-Rev. B	4K x 4	CMOS/epi (0.5 µm)	TIX	~5	5.0E+00						IPN	Duzellier, et al, 95IEEE TNS, No. 6, pg 1797. All "1s" @ high energy. High vs medium energy beam study. Comparison studies done at Saturne (France).
CNES	SMJ44100	4M x 1	CMOS/epi	TIX	<0.4			>2.4E-07	1992			IPN	Duzellier, et al, 93IEEE Wrkshp Rec. pg. 36. D/C ES. Proton data exists. See following entry.
IBM	SMJ44400	1M x 4	CMOS epi?	IBM					1990	16		BNL	Soft error data exists.
GSFC	TC5117400FT-70	4M x 4	CMOS	TOS					May-94			BNL	Pending analysis. LaBel
GSFC	TC5117400J-6	4M x 4	CMOS	TOS	<1.46	3.0E+00		1.8E-07		>100		BNL	LaBel, et al, 96IEEE TNS, No. 6, pg 2974. SEU cross section @ LET = 100. No stuck bits. No multiple errors. Vcc=5V.
ESA	TC514100Z-10	4M x 4	CMOS	TOS	~1			6.0E-07	Sep-91	>50		IPN	RADECS 91
JPL	**TC5165805AFT-50**	**8M x 8**	**CMOS**	**TOS**	**~1**	**1.0E-08**			**1998**			**BNL**	**Swift, RADECS98 preprint. D/C 9721. Cross section without row or column upsets.**
WU	TC51832p	DRAM	planar cell structure [cap & Xtr]	TOS	~2				Jul-96			WU	Matsukawa preprint. Data from He ion microprobe , IEEE, July 1996
GSFC	TMS416400	DRAM	CMOS	TIX	~2				Mar-97			BNL?	LaBel, et al, EEE Links, Vol. 3, No. 1, Mar 97, pg 5
ESA	TMS416400A (1992)	16M x 1	CMOS	TIX	<1		15		1995	>75	1.0E-04	BNL	Harboe-Sorensen, 95IEEE Wrkshp Rec., p 42. Row errors =1.0E-04 cm2/device. Strong preference for 1 to 0 transitions.
GSFC	TMS416400DJ-60	4M x 4	CMOS	TIX	3				Mar-97			BNL?	LaBel, et al, EEE Links, Vol. 3, No. 1, Mar 97, pg 5
GSFC	**TMS416400DJ-60**	**4M x 4**	**CMOS**	**TIX**	**<2.5**				**1996**	**>65**		**BNL**	**LaBel, et al, 97IEEE Wrkshp Rec., pg 14. Bit errors.**
CNES/ ALC	TMS416400-Rev. B	DRAM	CMOS/epi E848 (0.5 µm)	TIX	<<1.7	5.0E+00				>57		BNL & IPN	Calvel, 94IEEE TNS, No. 6, pg 2267. Loss of functionality @ LET = 25; 5.0E-05 cm^2. Full row error cross section = 1.0E-04 cm^2. Also half row errors.
ESA	TMS4416	16K x 4	NMOS	TIX	<5			2.0E-06	Dec-90			IPN	Harboe-Sorensen, et al, 90IEEE TNS, No. 6, pg. 1938.

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Test Org.*	Device	Function	Technology	Mfr.	Effective SEU LET* Threshold	Device Xsection (cm^2)	Bits Tested	Bit Xsection (cm^2)	Test Date	LUth	LU Xsection (cm^2)	Fac.	Remarks 31-Aug-99
Legend													
	Manufacturers: ATT - American Telephone & Telegraph; EDI - EDI Corp; FUJ - Fujitsu; HTC - Hitachi; IBM -IBM Federal Systems; INT - Intel; MCN - Micron Technologies; MIT - Mitsubishi; MOS - Mostek;												
	MOT - Motorola Semiconductors; NEC - Nippon Electric Corp; SAM - Samsung; SIE - Siemens; TIX - Texas Instruments; TOS - Toshiba												
	Test Organizations			**Radiation Test Facilities**									
	ALC - Alcatel Espace, France			BNL - Tandem Van de Graaff, Brookhaven National Laboratories, Long Island, NY									
	ARSP - Aerospace Corp., El Segundo, CA			CYC - CYCLONE, Université Catholique de Louvain-la-Neuve, Belgium									
	CERT - CERT-ONERA, France			IPN - Insitute Physique Nuclaire, University of Orsay, France									
	CNES - Centre National d'etudes Spatiales, Toulouse, France			IUCF - Indiana University Cyclotron Facility, Bloomington, IN									
	ESA - European Space Agency, Noordwijk, Netherlands			PSI - Paul Scheerer Institute, Villigen, Switzerland									
	GSFC - Goddard Space Flight Center, Greenbelt, MD			SAT - SATURNE, CEA, Saclay, France									
	IBM - IBM Federal Systems Division, Manassas, VA			TAM - Texas A&M University Cyclotron Institute, College Station, TX									
	JPL - Jet Propulsion Laboratory, Pasadena, CA			UCB - 88-inch Cyclotron, University of California, Berkeley, CA									
	LFS - Lockheed Federal Systems, Manassas, VA			UCD - University of California at Davis, Crocker Nuclear Laboratory, Davis, CA									
	NRL - Naval Research Laboratory, Washington, DC			UW - University of Washington cyclotron, Seattle, WA									
	ROCK - Rockwell Corp. (now Boeing), Anaheim, CA			WU - Waseda University, Japan									
	SEI - Space Electronics, Inc, San Diego, CA												
	SNL - Sandia National Laboratories, Albuquerque, NM												
	UW - University of Washington, Seattle, WA												