Test Org.*	Device	Function	Technology	Mfr.	Effective SEU LET* Threshold	Device Xsection (cm^2)	Bits Tested	Bit Xsection (cm^2)	Test Date	LUth	LU Xsection (cm^2)	Fac.	Remarks 30-Aug-99
		Gate Arrays/PALs/PLAs											
	Note: Entries in **RED** indicate data added since the 1997 Compendium.												
SEI	**10050LPRP**	**50K Gate Reprogram. PLA**	**CMOS**		**11**	**3.7E-03**			**1997**	**>25**	**3.2E-03**	**BNL**	**Layton, et al, 98IEEE Wrkshp Rec., pg 170.**
ESA/MMS	16L8	PLA	Bipolar IMPACT	TIX		1.3E-05			1993				H. Van Looy. ESA Rept. 1993
ESA	20RA10Z	Prog. Logic Device (PLD)	CMOS	SEQ		4.2E-05			Jun-91				Adams, ESA/ESTEC
IBM	22V10	PLA	CMOS	CYP	5	7.0E-06			1993	25	3.0E-04		Die sim ilar to below.
IBM	22V10	PLA	CMOS	MMI	5	1.0E-05			1993	25	3.0E-04		Die similar to above.
ESA/MMS	22V10	PLA	Bipolar IMPACT	TIX		2.0E-05			1993				H. Van Looy. ESA Rept. 1993
GSFC	22V10B-15	PLA	CMOS	CYP					Dec-92	<<26			Compare above & below.
GSFC	22V10C-10	PLA	BiCMOS	CYP	>120				Dec-92	>120			Compare below.
GSFC	22V10D-15DMB	PLA	CMOS	CYP					Dec-92	<<26			Compare above & below.
SEI	**22V10FRP**	**Reprogrammable PLA**	**CMOS**		**<11**	**7.5E-05**			**1997**	**>80**		**BNL**	**Layton, et al, 98IEEE Wrkshp Rec., pg 170.**
SEI	**22V10RP**	**PLA**	**CMOS**		**<3**	**4.5E-04**			**1997**	**>117**		**BNL**	**Layton, et al, 98IEEE Wrkshp Rec., pg 170.**
GSFC	**22V10RPFE**	**PLA**	**CMOS**	**SEI**	**<3.38**				**1997**	**>72.9**		**BNL**	**O'Bryan, et al, 98IEEE Wrkshp Rec., pg 39. D/Cs XC34908493, XC34950484, 002611202. F/F errors.**
GSFC	**22V10RPFE**	**PLA**	**CMOS**	**SEI**	**~10**				**1997**	**>72.9**		**BNL**	**O'Bryan, et al, 98IEEE Wrkshp Rec., pg 39. D/Cs XC34908493, XC34950484, 002611202. Combinatorial errors.**
GSFC	AT22V10	PLA	CMOS	ATM	~10	3.0E-05			Aug-93	>80			LaBel, et al, 94IEEE Wrkshp Rec., pg 64.
IBM	BTVCMOS2	SPD3 Gate Array	CMOS II (Burlington, VT)	IBM	3				Jan-93	25			LU rates given by J. Pollock of WP-2. Tested by T. Scott
JPL	CDI6007	Gate Array	CMOS	LED	>75				Jun-85				
IBM	CY7C344	PLD	CMOS	CYP					Apr-93				D/C 9305 Latchup rates given. WP-2 (Jim Pollack)
ARSP	EP1210	PLD	CMOS (4 µm feature)	ALT					Jun-88	>100			String of D-type F/F's.
ARSP	EP1800	PLD	CMOS (2 µm feature)	ALT					Jun-88	15	2.0E-03		String of D-type F/F's.
McD	EP1810	Electronically PLD	CMOS bulk	ALT	<4	1.0E-02			Sep-93	5	1.0E-03		W. Zakrzewski, (Also tested EP610)
ESA	EP310	Prog. Logic Device (PLD)	C/NMOS?	ALT	5.4	3.6E-05			1991				Adams, ESA/ESTEC.
ROCK	EP310DM	UVE Electronically PLD	C/NMOS	ALT	12	1.8E-04							
ESA	EP600	PLD	C/NMOS?	ALT	8	3.0E-06			Jun-91				Adams, ESA/ESTEC. Fab from Intel wafers may change.
ROCK	EP600DM	UVE Electronically PLD	C/NMOS	ALT	12	1.8E-04							
BREL/MCD	EP610	Electronically PLD	CMOS bulk	ALT					Oct-94	9	5.0E-04		Normand. D/C 9317, Temp = 44 to 100° C;

Heavy Ion SEE

Test Org.*	Device	Function	Technology	Mfr.	Effective SEU LET* Threshold	Device Xsection (cm^2)	Bits Tested	Bit Xsection (cm^2)	Test Date	LUth	LU Xsection (cm^2)	Fac.	Remarks 30-Aug-99
ARSP	EP910JC	UVE Electronically PLD	CMOS	ALT	4				Dec-89	15	7.0E-04		
PHY	EPM5032	UVE Electronically PLD	CMOS bulk	ALT					Mar-93	3	1.0E-03		Temp = 95° C. Rept. No. PHY-93R013
ARSP	HP03	Process Prog. GA	CMOS/epi	UTM	45				Dec-92	>80			Koga, et al, 92IEEE-TNS, No. 6, pg 1685.
HON	HR1060	Gate Array	RICMOS III	HON	22				Jun-91	>120			Test Metal had 4 functions tested.
JPL	HR1060	Gate Array (custom CDU)	RICMOS III	HON	60				Mar-92	>120			Up to 125° C. Same fab, different implementation as preceding
GSFC	HR2340	Gate Array (multifunction)	RICMOS IV	HON									Soft latch?
GSFC	**HX2300**	**SOI Test Metal**	**RICMOS SOI 4**	**HON**	**>120**				**1995**	**>120**			**LaBel, et al, 96IEEE Wrkshp Rec., pg 19.**
GSFC	**IMP50E10**	**Electrically Prog. Anal. Circ.**	**CMOS**	**IMP**	**1.45**				**1995**	**15 to 26.6**			**LaBel, et al, 96IEEE Wrkshp Rec., pg 19.**
JPL	LCA10038Q	Process Prog. GA	HCMOS/epi (10 µm.)-- not RLSI	HON	30				Jul-93	>115			Only 64-bit RAM tested.
HAC	LCA200K Process	ASIC Process test chip	200K series ASIC process	LSI					Mar-93	5	4.0E-02		Shoga. LU=5 @ 37° & 3.2 @ 60° C. LU doesn't damage device.
GD/ARSP	LL7320Q	Process Prog. GA	CMOS	LSI	20				Dec-88	25	1.0E-04	Cf-252	
JPL/ARSP	LRH10038Q	Process Prog. GA	HCMOS/epi	LSI	30				Dec-88	>120			
LSI	LRH20K	PPGA Evaluation Device	Rad Hard HCMOS/epi	LSI	30	1.0E-06			Dec-92	>200			Owens, 92IEEE Wrkshp Rec., p 67. Config. as 1K SRAM.
ARSP	LRH91000	Process Prog. GA	CMOS/epi	LSI	50				Mar-90	>100			
ARSP	LRH9320Q	Process Prog. GA	Rad Hard HCMOS/epi	LSI	30				Dec-88	>120			Only 64-bit RAM tested
CNES	MB5000	Mem. Plan. GA	HCMOS/epi	MHS	30	5.0E-03			Nov-90				Chapuis. ESA Conf.
JPL	MB5000	Mem. Plan. GA	HCMOS/epi (10 µm)	MHS	40	5.0E-03			Aug-87				Tested as 256x7 RAM.
JPL	MB5000	Mem. Plan. GA	HCMOS/epi (8 µm)	MHS	25				Nov-87				Tested as 256x7 RAM.
MMS	MC Family	Gate Array	Rad Tol. 1 µm. SuperCMOS	MHS	32				Dec-90	>115			
MMS	MC5000	Gate Array 35K	SCMOS/epi RT	MHS					1992	>80			Dufour, 92IEEE Wrkshp Rec., pg 21.
SOR	PAL16R8BMJ/883B	PLA	Bipolar (two parts)	AMD	7	2.5E-04			1993				J. Barak, et al, 93IEEE Wrkshp Rec., pg 33. Test 8-bit reg. All "1s" worst case.
ARSP	PAL22V10A	PLA	Bipolar	AMD	4				Jun-92				
ARSP	PAL22V10A	PLA	Bipolar	TIX	4				Jun-92				
ARSP	PALC22V10B	PLA	CMOS	CYP	5				Dec-92	12	5.0E-04		
ARSP	RA20K	Process Prog. GA	CMOS/epi	UTM	55				Mar-92	>120			Koga, et al, 92IEEE TNS, pg 1685. D-type F/F & SRAM.
IBM	RHCMOS2	Expressway GA	CMOS	IBM	>6				Jan-93	>120			T. Scott, IBM Letter
MMS	TIBPAL16R8	PLA	Bipolar	TIX	9				Jul-94	>140			Beaucour,et al, 93IEEE Workshop, pg 20.

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Test Org.*	Device	Function	Technology	Mfr.	Effective SEU LET* Threshold	Device Xsection (cm^2)	Bits Tested	Bit Xsection (cm^2)	Test Date	LUth	LU Xsection (cm^2)	Fac.	Remarks 30-Aug-99
MMS	TIBPAL22V10	PLA	Bipolar	TIX	9				Jul-94	>140			Beaucour,et al, 93IEEE Workshop, pg 20.
GSFC	UT22VP10	PLA or PAL	CMOS 1.2 µm feature. RADPAL	UTM	~60				Nov-96	>109		UCB	Amorphous Si based. Katz, EEE Links, summarizes Boeing data.
GSFC	UT22VP10	RADPAL	——	UTM	37					>90		BNL	LaBel, et al, 96IEEE Wrkshp Rec., pg 19.
UTM	UTD-R RA212	Gate Array	CMOS/epi (1.5µm feature)	UTM	55	7.0E-05							UTM says data apply to all UTD-R family
UTM	UTE-R 50K	Gate Array	CMOS/epi (5 µm)	UTM	~36				Jun-93	>165			
UTM	UTE-R 75K	Gate Array	CMOS/epi (3 metal overlayer)	UTM	0.36								Runaway in F/F support circuitry. D. Nichols observed P. Rudeck's test
JH		Gate Array	ECL. (1.0 & 1.5 µm feature sizes)	ASD	<1.4				Apr-90				1 & 1.5 µm feature sizes. 50 MHz.
JH		Gate Array as FIFO	rad-hard CMOS	UTM					Jul-92	>162			Kinnison, 92IEEE Wrkshp Rec., pg 12.

Legend

Manufacturers: AMD - Advanced Micro Devices; CYP - Cypress Semiconductor; IDT - Integrated Device Technology; MMI - Monolithic Memories; MHS - Matra Harris Semiconductor; NSC - National Semiconductor; SRT - Saratoga Semiconductor

Test Organizations

ARSP - Aerospace Corp., El Segundo, CA
BREL - Boeing Radiation Effects Laboratory, Seattle, WA
CNES - Centre National d'etudes Spatiales, Toulouse, France
ESA - European Space Agency, Noordwijk, Netherlands
GSFC - Goddard Space Flight Center, Greenbelt, MD
HAC - Hughes Aircraft Co, El Segundo, CA
HAR - Harris Corp, Melbourne, FL
HON - Honeywell Space Systems, Clearwater, FL
IBM - IBM Federal Systems Division, Manassas, VA
JH - Johns Hopkins Applied Physics Lab, Laurel, MD
JPL - Jet Propulsion Laboratory, Pasadena, CA
LSI - LSI Logic, Milpitas CA
LMC - Lockheed-Martin Corp, Sunnyvale, CA
McD - McDonald-Douglas, Newport Beach, CA
MMS - Matra Marconi Space, France
ROCK - Rockwell Corp. (now Boeing), Anaheim, CA
SEI - Space Electronics, Inc, San Diego, CA
SOR - Soreq NRC, Israel
UTM - United Technologies Microelectronics Center, Colorada Springs, CO

Radiation Test Facilities

BNL - Tandem Van de Graaff, Brookhaven National Laboratories, Long Island, NY
CYC - CYCLONE, Université Catholique de Louvain-la-Neuve, Belgium
IUCF - Indiana University Cyclotron Facility, Bloomington, IN
TAM - Texas A&M University Cyclotron Institute, College Station, TX
TSL - The Svedberg Laboratory, Uppsala, Sweden
UCB - 88-inch Cyclotron, University of California, Berkeley, CA
UCD - University of California at Davis, Crocker Nuclear Laboratory, Davis, CA