Test Org.*		Function		Mfr.	Effective Threshold	Xsection (cm^2)	Bits	Xsection cm^2	Test	LUth	cm^2	Fac.	23-Aug-99
		Microprocessor (32-bit)											
	Note: Entries in **RED** indicate data added since the 1997 Compendium.												
CNES	68020		CMOS/epi	MOT	<1.7	1.0E-02			Jul-91	>54		IPN	Velazco, et al, 92IEEE Wrkshp Rec., pg.16. Register test
CNES	68020		CMOS/bulk	MOT	<1.7	1.0E-02			Jul-91	8	1.0E-02	IPN	Velazco, et al, 92IEEE Wrkshp Rec., pg.16. Register test
JH	68020		CMOS	MOT					1989	<40		Cf-252	Kinnison. See later data by CNES
JH	68020		CMOS/epi (15 µm)	MOT						<40		Cf-252 BNL	
JH	68020		CMOS/epi (12 µm) 1.35 µm features.	MOT						>50		Cf-252 BNL	
LIN	68020		CMOS/epi	MOT					Apr-91	32		BNL	
JPL	80386		CMOS	AMD	>>2.5				Jul-91	<24			
ARSP	68HC811		CMOS	MOT	3	3.0E-03			1995	8	8.0E-03	UCB	Koga
CNES	68T020		CMOS-SOI-0.8 µm (HSOI4CB)	TMS	7	1.1E-03	697		1994	>72		IPN	Lestrat, et al, 94IEEE TNS, No. 6, pg 2240. X-section = 2.4E-03 @ LET = 72.
JPL	**6x86-PR166+GP**	**166 MHz Pentium**	**CMOS**	**CYR**	**1.7**	**1.0E-04**			**Dec-97**			**TAM**	**JPL internal report. Cross section at LET = 37.**
NRL	79R3081	RISC	CEMOS-5 (6,8,10,12 µm epi)	IDT						12 to > 60	4.0E-03	BNL	Lestrat, et al, 94IEEE TNS, No. 6, pg 2240. LU = 12; 2.4E-03 @ LET = 72.
MMS	7C601	SPARC	CMOS bulk (0.8 µm)	CYP					1993	10	1.8E-02	GANIL	Beaucour, et al, 93IEEE Wrkshp Rec. pg. 20.
JPL	80386DX		CMOS/epi (CHMOS III)	INT			4000	6.0E-07	Jul-88	>40		UCB	EAX register only.
IBM	80386DX		CMOS/epi (CHMOS III)	INT	6			~1.0E-06	Apr-89		1.0E-05	Cf-252	BNL, proton & alpha SEU tests also negative
IBM	80386DX		CMOS/epi (CHMOS IV)	INT	6			~1.0E-06	Apr-89		1.0E-05	Cf-252	Same as above, except CHMOS IV latched up. Also proton upsets
JPL	80386DX		CMOS/epi (CHMOS IV)	INT	2.5 to 4.5		272	~1.0E-06	May-91	40		BNL	
JPL	80386DX		CMOS/epi (CHMOS III)	INT			~60		Jul-88	>40		UCB	EAX register only.
IBM	80386DX		CMOS/epi (CHMOS III)	INT	6		~100		Apr-89			Cf-252	BNL, proton & alpha SEU tests also negative.
IBM	80386DX		CHMOS IV	INT	6		~100				1.5E-05	BNL	Also proton upsets.
JPL	80386DX		CHMOS IV	INT	2.5 to 4.5		~100		May-91	40		BNL	R. Watson et al.
GSFC	80386DX-20B & -25		CHMOS IV	INT	3.4	1.0E-03			Apr-95	29	1.0E-04	BNL	Moran, et al, RADECS 95, pg 263. Nondestructive LU.
GSFC	80486DX2-66		CHMOS V (0.8 µm)	INT	~5	2.0E-04			1995	>90		BNL	Moran, et al, RADECS 95, pg 263. X-section with cache disabled. MicroLU @ LET > 20; < 1.0E-04 cm^2. Proton data also exists.
SEI	**80486DX2RP**	**50 MHz test frequency**	**CHMOS V (0.8 µm) 5.0 V**	**INT**	**<5.4**	**2.0E-03**			**1997**	**>40**		**BNL**	**Layton, et al, 98IEEE Wrkshp Rec., pg 170. D/C 9527527C. Cache on.**
SEI	**80486DX2RP**	**50 MHz test frequency**	**CHMOS V (0.8 µm) 5.0 V**	**INT**	**<5.4**	**1.5E-04**			**1997**	**>40**		**BNL**	**Layton, et al, 98IEEE Wrkshp Rec., pg 170. D/C 9527527C. Cache off.**
GSFC	80486DX-33		CHMOS IV (1.0 µm)	INT	~3	2.0E-04			1995	20		BNL	Moran, et al, RADECS 95, pg 263. X-section w/cache enabled. LU is catastrophic.

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Test Org.*	Device	Function	Technology	Mfr.	Effective SEU LET* Threshold	Device Xsection (cm^2)	Bits Tested	Bit Xsection (cm^2)	Test Date	LUth	LU Xsection (cm^2)	Fac.	Remarks 23-Aug-99
GSFC	80486DX-33		CHMOS IV (1.0 µm)	INT	5	~5.0E-05			1995	20		BNL	Same as above, x-section for cache disabled. Proton data exists.
JSC	**80486DX4**		**3LM CMOS [3.45V] 0.5 µm. Feature size.**	**AMD**	**1.5**	**2.5E-03**			**1996**	**~5**		**TAM**	**Kouba & Choi, Test Report 12/30/96 & 97IEEE Wrkshp Rec., pg 48. Threshold/X-sect with cache enabled. X-sect unsat. @ LET = 25. 8 error modes seen.**
JSC	**80486DX4**		**3LM CMOS [3.45V] 0.5 µm. Feature size.**	**AMD**	**4.5**	**2.5E-03**			**1996**	**~5**		**TAM**	**Same as above except threshold/cross section is for cache disabled .**
JSC	80486DX4		BiCMOS [3.3V] 0.6 µm feature size	INT	3.5	3.0E-04				~40		TAM	Kouba & Choi, Test Report 12/30/96. Threshold/cross section with cache enabled. Eight error modes seen.
JSC	80486DX4		BiCMOS [3.3V] 0.6 µm feature size	INT	6.5	3.0E-05				~40		TAM	Same as above except threshold/cross section is for cache disabled .
HAC	80960MX		CMOS	INT					Mar-93	15	1.0E-03	UCB	Two LU modes: 30 & 100's of mA. Shoga
CNES	90C601 SPARC601	SPARC	CMOS/bulk	MHS	2	8.0E-03				<13	2.0E-03	IPN Cf. 252	Estreme et al, 93IEEE Wrkshp Rec., pg 13. Registers only.
GSFC	**H30466A-21**		**CHMOS IV**	**SEI**	**5 to 6**				**1995**	**35 to 37.5**		**BNL**	**LaBel, et al, 96IEEE Wrkshp Rec., pg 19. MicroLU only. Count error cleared by reset.**
GSFC	**H30466A-21**		**CHMOS IV**	**SEI**	**3.4 to 5**				**1995**	**35 to 37.5**		**BNL**	**LaBel, et al, 96IEEE Wrkshp Rec., pg 19. MicroLU only. Reset errors.**
GSFC	**H30466A-21**		**CHMOS IV**	**SEI**	**6 to 11.4**				**1995**	**35 to 37.5**		**BNL**	**LaBel, et al, 96IEEE Wrkshp Rec., pg 19. MicroLU only. Lockup cleared by reset.**
JPL	**K5-PR166ABX**	**166 MHz Pentium**	**CMOS (3.5 V)**	**AMD**	**<0.4**	**6.3E-08**			**Jun-97**	**0.37**	**1.30E-06**	**BNL**	**Sat. LU x-section ~1.0E-01 cm^2. LU destructive.**
JPL	**K5-PR166ABX**	**166 MHz Pentium**	**CMOS (3.5 V)**	**AMD**	**<1.7**	**6.3E-08**			**Dec-97**	**1.7**	**~1.0E-06**	**BNL**	**Sat. LU x-section ~2.0E-03 cm^2. LU destructive.**
MMS	L64730	DCT processor	CMOS	LSI						8	2.0E-03	GANIL	Beaucour, et al, 93IEEE Wrkshp Rec. pg. 20.
JPL	L64801	Integer unit (SPARC)	"rad-hard" CMOS/epi (10 µm)	LSI	7	2.0E-05			Mar-94	15	8.0E-04	BNL	LU cross section @ LET = 60. See MMS data
MMS	L64811	SPARC	CMOS	LSI						8	5.0E-02	GANIL	Dufour, et al, 92IEEE Wrkshp Rec., pg 21..
CNES	L64811	SPARC	CMOS	LSI	2	2.0E-03			1993	~4	5.0E-02	IPN	Estreme et al, 93IEEE Wrkshp Rec., pg 13. Registers & applications
GSFC	**MG80486DX2-66**		**CHMOS IV**	**INT**	**4.3 to 7.9**				**1997**	**26.6 to 37.3**		**BNL**	**O'Bryan, et al, 98IEEE Wrkshp Rec., pg 39. D/C 9451. Dynamic tests with and without cache enabled. Both data and lockup SEUs observed. Also microlatches and destructive SEL @ LET >26.6**
GSFC	Mongoose (R3000)	RISC	HCMOS/epi (1.0 µm)	LSI	23	4.0E-05			Apr-93	>85		BNL	LaBel, et al, 94IEEE Wrkshp Rec., pg 64. A RH version of R3000-based 'Cobra"
GSFC	**Mongoose V (R3000)**	**RISC**	**CMOS/SOI (Honeywell)**	**SYN**	**>83**				**1997**	**>96**		**BNL**	**O'Bryan, et al, 98IEEE Wrkshp Rec., pg 39. No cache.**
GSFC	**Mongoose V (R3000)**	**RISC**	**CMOS/SOI (Honeywell)**	**SYN**	**~40**				**1997**	**>96**		**BNL**	**O'Bryan, et al, 98IEEE Wrkshp Rec., pg 39. Cache on**
GSFC	**MQ80386-25/B**		**CHMOS IV**	**INT**	**4 to 5**	**8.0E-05**				**30 to 32**		**BNL**	**LaBel, et al, 96IEEE Wrkshp Rec., pg 19. MicroLU only. Count or lockup cleared by reset.**
GSFC	**MQ80386-25/B**		**CHMOS IV**	**INT**	**5 to 6**	**1.5E-03**				**30 to 32**		**BNL**	**LaBel, et al, 96IEEE Wrkshp Rec., pg 19 . MicroLU only. Lockup cleared by power reset.**
LLNL	PR3400	RISC	CMOS PACE III (0.6 µm)	PFS	<3	1.0E-03				14 to 24	1.0E-04	UCB	J. Kimbrough, et al, 94IEEE TNS, No. 6, Pt II, p. 2706.
LLNL	PR3400A	RISC	CMOS PACE II (0.7 µm)	PFS	<3	1.0E-03				38 to 63	1.0E-05	UCB	J. Kimbrough, et al, 94IEEE TNS, No. 6, Pt II, p. 2706.
LLNL	PR3400L	RISC	CMOS PACE III (0.6 µm)	PFS	<3	1.0E-03				14 to 24	1.0E-04	UCB	J. Kimbrough, et al, 94IEEE TNS, No. 6, Pt II, p. 2706.

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Test Org.*	Device	Function	Technology	Mfr.	Effective SEU LET* Threshold	Device Xsection (cm^2)	Bits Tested	Bit Xsection (cm^2)	Test Date	LUth	LU Xsection (cm^2)	Fac.	Remarks 23-Aug-99
HAR	R3000	RISC	CMOS	IDT					May-91	4.8		BNL	VLSI MIPS RISC. D. Vail (HAR)
ESA	R3000	RISC	CEMOS IV	IDT			736		1992	<3.3		BNL	Harboe-Sorensen, et al, 92IEEE Wrkshp Rec., pg 34.
HAR	R3000	RISC	CMOS	LSI					May-91	53		BNL	VLSI MIPS RISC. D. Vail (HAR)
ESA	R3000	RISC	CMOS	LSI	~3		736	3.0E-06	1992	>60		BNL	Harboe-Sorensen, et al, 92IEEE Wrkshp Rec., pg 34.
ESA	R3000	RISC	CMOS	NEC	<10		736		1992	60		BNL	Harboe-Sorensen, et al, 92IEEE Wrkshp Rec., pg 34.
HAR	R3000	RISC	Adv. CMOS	PFS	<3.4	1.0E-03	~1300		May-91	>120		BNL	VLSI MIPS RISC. D. Vail (HAR)
ESA	R3000	RISC	PACE I	PFS	~6		736	1.0E-06	1992	>60		BNL	Harboe-Sorensen, et al, 92IEEE Wrkshp Rec., pg 34.
HAR	R3000	RISC	Adv. CMOS	SIE	6	1.0E-03	~1300		May-91	>120		BNL	VLSI MIPS RISC. D. Vail (HAR)
ESA	R3000	RISC	Adv. CMOS	SIE	<10		736	1.0E-06	1992	>60		BNL	Harboe-Sorensen, et al, 92IEEE Wrkshp Rec., pg 34.
HAR	R3000A	RISC	CMOS	IDT					May-91	26		BNL	VLSI MIPS RISC. D. Vail (HAR)
ESA	R3000A	RISC	CEMOS V	IDT	~6		736	>1.0E-06	1992	27		BNL	Harboe-Sorensen, et al, 92IEEE Wrkshp Rec., pg 34.
LLNL	R3000A	RISC	CMOS 6 (0.8 µm)	IDT	~5	1.0E-03				14 to 24	2.0E-04	UCB	J. Kimbrough, et al, 94IEEE TNS, No. 6, Pt II, p. 2706.
ESA	R3000A	RISC	HCMOS	LSI	<8		736	1.0E-06	1992	60		BNL	Harboe-Sorensen, et al, 92IEEE Wrkshp Rec., pg 34.
LLNL	R3000A	RISC	CMOS (0.7 µm)	LSI	<2.8	2.0E-03				38 to 63	2.0E-05	UCB	J. Kimbrough, et al, 94IEEE TNS, No. 6, Pt II, p. 2706.
LLNL	R3000A	RISC	CMOS	NEC	3	1.0E-03			Dec-94	38 to 63	6.0E-04	UCB	J. Kimbrough, et al, 94IEEE TNS, No. 6, Pt II, p. 2706.
HAR	R3000A	RISC	CMOS?	PFS					May-91	60		BNL	VLSI MIPS RISC. D. Vail (HAR)
ESA	R3000A	RISC	CMOS PACE II	PFS	<6		736	1.2E-06	1992	>60		BNL	Harboe-Sorensen, et al, 92IEEE Wrkshp Rec., pg 34.
LLNL	R3000A	RISC	CMOS PACE III (0.6 µm)	PFS	<3	2.0E-03			Dec-94	>63		UCB	J. Kimbrough, et al, 94IEEE TNS, No. 6, Pt II, p. 2706.
ESA	R3000A	RISC	Adv. CMOS	SIE	~6		736	2.0E-06	1992	>60		BNL	Harboe-Sorensen, et al, 92IEEE Wrkshp Rec., pg 34.
LLNL	R3000A	RISC	CMOS	SIE	4	2.0E-03			Dec-94	>63		UCB	J. Kimbrough, et al, 94IEEE TNS, No. 6, Pt II, p. 2706.
LLNL	R33000HC	RISC	CMOS-- 1.0 µm.	LSI	3	5.0E-03			Dec-94	24 to 38		UCB	J. Kimbrough, et al, 94IEEE TNS, No. 6, Pt II, p. 2706.
IBM	RAD6000 FIxed Point		RHCMOS-E [CMOS/epi]	LFSC	15			1.2E-07	Jan-93	>120		BNL	Haddad. T > 120 deg C. FXPT chip (1 of 5 chips) simulates RH RSC6000.
HON	**RH-32**	**RISC**	**Honeywell HI Process**	**HON**	**~30**			**4.6E-07**	**1997**	**>83**		**BNL**	**Leavy, et al, 98IEEE Wrkshp Rec., pg 11.**
ESA	T414		CMOS/epi	ISM	3	2.0E-01	16K	2.0E-06				HARW	No latchup. Also tested with Cf-252.
ESA	T414		CMOS/bulk	ISM	3	2.0E-01	16K	2.0E-06				HARW	Latchup of on-chip RAM. Also tested with Cf-252.
MMS	T800	Transputer (32-bit)	CMOS	ISM						45	>1E-4	GANIL	
CNES	T805	Transputer (32-bit)	CMOS	ISM	~2			1.0E-05	1995	36		IPN	Bezerra, RADECS 95, pg 340. Register bit cross section (static). Dynamic = short applications; static = register

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Test Org.*	Device	Function	Technology	Mfr.	Effective SEU LET* Threshold	Device Xsection (cm^2)	Bits Tested	Bit Xsection (cm^2)	Test Date	LUth	LU Xsection (cm^2)	Fac.	Remarks 23-Aug-99
CNES	T805	Transputer (32-bit)	CMOS	ISM	~2			5.0E-06	1995	36		IPN	Bezerra, RADECS 95, pg 340 Cache bit cross section. Worst case is dynamic test with cache enabled.
ARSP	XC6802		CMOS	MOT					1994			UCB	Koga
ARSP	XC68302		CMOS	MOT	3	5.0E-04			1994	15	6.0E-03	UCB	Koga
Legend													
	Manufacturers: AMD - Advanced Microdevices; CYP - Cypress; HON - Honeywell; IDT - Integrated Device Technology; INT - Intel; ISM - Inmos Corp; LFSC - Lockheed-Martin Federal Sustems; LSI - LSI Logic, Inc;												
	MHS - Matra Harris Semiconductor; MOT - Motorola Semiconductor Division; NEC - Nippon Electric Corp; PFS - Performance Semiconductor; SEI - Space Electronics, Inc; SIE - Siemens; SYN - Synova; TMS - Thompson Military & Space (France)												
	Test Organizations			**Radiation Test Facilities**									
	ARSP - Aerospace Corp., El Segundo, CA			BNL - Tandem Van de Graaff, Brookhaven National Laboratories, Long Island, NY									
	CNES - Centre National d'etudes Spatiales, Toulouse, France			Cf-252 - Cf-252 Fission Source (various facilities)									
	ESA - European Space Agency, Noordwijk, Netherlands			GANIL - GANIL Accelerator, France									
	GSFC - Goddard Space Flight Center, Greenbelt, MD			HARW - Harwell Laboratory, Oxford, UK									
	HAC - Hughes Aircraft Co, El Segundo, CA			IPN - Insitute Physique Nuclaire, University of Orsay, France									
	HAR - Harris Corp, Melbourne, FL			IUCF - Indiana University Cyclotron Facility, Bloomington, IN									
	HON - Honeywell Space Systems, Clearwater, FL			TAM - Texas A&M University Cyclotron Institute, College Station, TX									
	IBM - IBM Federal Systems Division, Manassas, VA			UCB - 88-inch Cyclotron, University of California, Berkeley, CA									
	JPL - Jet Propulsion Laboratory, Pasadena, CA												
	JSC - Johnson Space Flight Center, Houston, TX												
	LIN - MIT Lincoln Labs, Lexington, MA												
	LLNL - Livermore National Laboratories, Livermore, CA												
	MMS - Matra Marconi Space, France												
	NRL - Naval Research Laboratory, Washington, DC												
	SEI - Space Electronics, Inc, San Diego, CA												