Test Org.*	Device	Function	Technology	Mfr.	Effective SEU LET* Threshold	Device Xsection (cm^2)	Bits Tested	Bit Xsection (cm^2)	Test Date	LUth	LU Xsection (cm^2)	Fac.	Remarks 31-Aug-99
	Note: Entries in **RED** indicate data added since the 1997 Compendium.												
		Analog Switches/MUXs											
GSFC	**1840RP**	**16-channel analog MUX**	**CMOS**	**SEI**	**>110**				**1997**			**BNL**	**O'Bryan, et al, 98IEEE Wrkshp Rec., pg 39.**
ARSP	54ACT253	Dual, 4-channel, 3-state MUX	ACMOST/epi	NSC					May-90				
JPL	DG125AP	Analog Switch	CMOS/epi	SIL					Jan-88	>120			At T = 125 °C
JPL	DG125BP	Analog Switch	CMOS/epi	SIL					Jan-88	>120			At T = 125 °C
BREL	DG201(M38510)	Quad SPST (w/drivers)	Unknown	HAR					May-93	>38			W. Will (WP-01). D/C 9218.
BREL	DG201(M38510)	Quad SPST (w/drivers)	Unknown	SIL					May-93	>38			W. Will (WP-01) D/C 9125. .
MMS	DG271	Quad SPST (w/drivers)	CMOS	SIL					1992	>137			Dufour, et al, 92IEEE Workshop Record, pg. 21.
MMS	DG300	Dual SPST (w/drivers)	CMOS	SIL					1992	>137			Dufour, et al, 92IEEE Workshop Record, pg. 21.
JPL	DG303	Dual SPST (w/drivers)	CMOS/epi	SIL					Jan-88	>120			At T = 125 °C
JPL	DG507	8-channel differential MUX	CMOS/epi	SIL					Dec-87	>120			At T = 75 °C
BREL	DG507AAK/883	8-channel differential MUX	Unknown	SIL					May-93	>38			W. Will (WP-01). D/C 9134.
ARSP	DG601AK	Quad SPST MUX	CMOS/epi [13 µm.]	SIL					Jun-92	>100			
ARSP	HI546	16-channel MUX	CMOS	HAR					Mar-88	>60		UCB	No latchup at at T=60 C°.
ARSP	HI548	8-channel MUX	CMOS	HAR					Mar-88	>60		UCB	No latchup at at T=60 C°.
ARSP	HI549	4-channel differential MUX	CMOS	HAR					Mar-88	>60		UCB	No latchup at at T=60 C°.
GSFC	HS508RH	8-channel Rad-hard MUX	HCMOS	HAR	110				Jun-93	>100		BNL	LaBel, et al, 94IEEE Workshop Record, pg. 64.
ARSP	IH6208	8-channel analog MUX	CMOS	HAR					1992	>100			
		ASICs											
NRL	388052	ASIC		LIT					Feb-93	<<29.5	1.0E-03	BNL	Limited LU test. Stapor memo for test of Feb 93.
SEI	**65C02**	**ASIC process test**	**CMOS Fab 1**	**SEI**	**>23 <37**	**1.5E-04**			**Mar-97 Feb-97**	**>120**		**BNL UCD**	**Layton, et al, 98IEEE Wrkshp Rec., pg 170.**
GSFC	Bus Contoller	Bus	standard CMOS/epi	MHS	<11.5	1.5E-05			Jul-92	>87			LaBel. Fairchild-designed
JPL	CD54HC4046	Phase Lock Loop	HCMOS/bulk-3.0 µm.	HAR					Apr-95	>120		BNL	
CNES	ES 10050		CMOS/epi (12 µm)	ES2					Dec-90	25	1.0E-04		Chapuis, et al, 90IEEE TNS, No. 6, pg. 1839. D/C 9016.
CNES	MACS TC02	MACS Bus Controller	MA Gate Array	MHS	110	3.0E-06			1992	>124			Dufour, et al, 92IEEE Wrkshp Rec., pg 21.
MMS	MB5000		CMOS 8µm./10µm.	MHS	30	5.0E-03			1992	>62			Dufour, et al, 92IEEE Wrkshp Rec., pg 21.
ARSP	Q3216 & Q3236	ASIC	Phase Lock Loop-BiCMOS	QLC	1	1.0E-04				>65		UCB	Jobe, et. al., 96IEEE TNS, No. 6, pg 2868. Phase upset.

Test Org.*	Device	Function	Technology	Mfr.	Effective SEU LET* Threshold	Device Xsection (cm^2)	Bits Tested	Bit Xsection (cm^2)	Test Date	LUth	LU Xsection (cm^2)	Fac.	Remarks 31-Aug-99
	Note: Entries in **RED** indicate data added since the 1997 Compendium.												
ARSP	Q3216 & Q3236	ASIC	Phase Lock Loop-BiCMOS	QLC	1	3.0E-04				>65		UCB	Jobe, et. al., 96IEEE TNS, No. 6, pg 2868. Frequency upset.
NRL	QL12X16	ASIC (larger than QL8X12)		QLC								UCD	Stapor. Proton test - No LU or SEU @ 63MeV. Implies H.I. LETth > 8. 25 mHz.
NRL	QL8X12	ASIC		QLC	12	1.5E-02				12	1.5E-02		Stapor. LU & SEU have same threshold & X-section. LU current >800 mA. 25 mHz.
GSFC	Serial Controller		standard CMOS/epi	MHS	4.5	4.0E-05			Jul-92	>87			
		ADC (6-bit)											
A	MP7682		CMOS	MPS					Jul-89				
		ADC (8-bit)											
GSFC	7820RP/372		LCCMOS (Seiko 0820 die)	MPS					Jul-94	>80			LaBel
GSFC	**AD570**	**Sucessive Approximation**	**CMOS**	**ADI**	**7**	**3.0E-04**			**1996**	**>52.5**		**BNL**	**LaBel, et al, 97IEEE Wrkshp Rec., pg 14.**
BREL	AD7824		CMOS	ADI	<<5	1.0E-04			Feb-91				Fluorine only
ARSP	AD9048	Flash	Bipolar	ADI	<1	3.0E-04			1994				Koga, 94IEEE TNS, pg 2172. D/C 9146. Fail to 2's complement @ LET = 8; 1.5E-05 cm^2.
HON	AD9048TQ	Flash	Bipolar	ADI	<<3	3.2E-04							Fail LET = 7; 1.3E-05 cm^2. Unexplained high currents
JPL	**HI1276**	**Flash**	**ECL (Bipolar)**	**HAR**					**Mar-97**	**>70**		**BNL**	**Temp. increased from ~32° C to 69° C during test.**
JPL	HI1276	Flash	Bipolar- ECL	HAR					Mar-97	>70		BNL	With self heating up to T = 69 °C.
SNL	HS9008RH	Flash	CMOS	HAR	~15	2.0E-05			1994	>150			Sexton, et al, 94IEEE Wrkshp Rec., pg 55. Up to T = 125° C.
GD	MP7683	Flash	CMOS	MPS		4.0E-06							
SEI	**MP7684**	**20 MSPS**	**CMOS**	**EXR**	**<11.4**	**6.0E-02**			**1997**	**18 - 26.6**		**BNL**	**Layton, et al, 98IEEE Wrkshp Rec., pg 170.**
ARSP	MP7684		CMOS	MPS	~1	1.0E-03			Dec-91	>100			
JPL	MP7684	Flash	CMOS	MPS					Nov-92	>120			Up to 125° C.
JPL	MP7684A	Flash	CMOS	MPS					Nov-92	>120			Up to 125° C.
JPL	SPT7725	Flash	CMOS	SPT					Mar-97	>120		BNL	Used thermo-electric cooler to maintain temp < 34 °C.
ARSP	TDC1048		Bipolar hybrid	TRW	2	2.0E-03			Apr-93	>95			D/C 8540
JPL	TDC1048J6A		Bipolar hybrid	TRW	~5				Nov-89	>95			T=96° C. Same SEU as adjacent part.
JPL	TDC1048J6C		Bipolar hybrid	TRW	~5				Nov-89	>95			T=96° C. Same SEU as adjacent part.
NRL	TMC1175	Flash	CMOS	TRW					Feb-93	<<29.5	2.0E+04	BNL	Limited LU test. Stapor memo.
JPL	**TMC1175C3V20**	**Video Flash**	**Submicron CMOS**	**RAY**					**Jun-97**	**25**	**1.1E-04**	**BNL**	**LU rate (GCR) = 5E-03/yr.**
CNES	TMS8338		CMOS (HS13)	TMS					Aug-91	~20	5.0E-04		See following entry.

Test Org.*	Device	Function	Technology	Mfr.	Effective SEU LET* Threshold	Device Xsection (cm^2)	Bits Tested	Bit Xsection (cm^2)	Test Date	LUth	LU Xsection (cm^2)	Fac.	Remarks 31-Aug-99
	Note: Entries in **RED** indicate data added since the 1997 Compendium.												
CNES	TMS8338		CMOS (HCMOS3)	TMS					Aug-91	~12	2.0E-03		See preceding entry.
		ADC (10-bit)											
JPL	AD573	Internal reference.	Bipolar-IIL	ADI					Nov-89	>110		UCB	
JPL	AD773A		BiCMOS	ADI					Sep-96	>120		BNL	Up to 70 deg. C, @ 5.25V.
	ADC10061CMJ	Flash		NSC		8.0E-05				11	1.0E-06		
ARSP	MP7695	Parallel output.	CMOS	MPS					Jun-92	>100			
		ADC (12-bit)											
JPL	AD12062		CMOS/epi	ADI					Mar-97	12	3.0E-04	BNL	Unsat. @ LET = 60. Cross section plot exists.
GSFC	AD1671JD	Internal reference, parallel out	Bipolar/CMOS	ADI					Apr-93	>90			LaBel, et al, 94IEEE Wrkshp Rec., pg 64. D/C 9219.
NSWC/ ARSP	AD42961	Hard AD871	RBCMOS = RH BiCMOS	ADI	3	4.8E-03			1994	>126			Turflinger, 94IEEE TNS, No. 6, pg 2187. Noise cross section also exists.
NSWC/ ARSP	AD42961	Flash. (hard AD871)	RBCMOS = RH BiCMOS	ADI	~10	1.0E-05			Apr-96	>126		UCB.	Turflinger, 94IEEE TNS, No. 6, pg 2187. Offset errors. Division by samples per irradiation recommended.
NSWC/ ARSP	AD42961	Flash. (hard AD871)	RBCMOS = RH BiCMOS	ADI		5.0E-05			Apr-96	>126		UCB.	Turflinger, 94IEEE TNS, No. 6, pg 2187. Noise errors. Division by samples per irradiation recommended.
JPL	AD574A	Internal reference	BiMOS	ADI	<3				Sep-91	>120			
JPL	AD574A	Internal reference	BiMOS	ADI	<3	1.5E-04			Sep-91	>110		UCB	8 MSBs tested.
JPL	AD674A	Internal reference	Bipolar hybrid	ADI	<3	---			Sep-91	>120			
JPL	AD674B	Internal reference, parallel out	BIMOS II	ADI	<3	5.0E-04			Nov-92	>120			
JH	AD7672	Parallel and serial output	CMOS	ADI					Jan-91	>75			Kinnison
JPL	AD7672B	Parallel and serial output	CMOS	ADI	6				Sep-91	>175			Kinnison
JPL	AD7870	Internal reference	LC^2MOS non-hard	ADI					1995	>120			Nichols, et. al., 95IEEE Wrkshp Rec., pg 1. Tested up to 60 °C.
SNL	AD7876	Parallel; two 8-bit bytes; or serial	LC^2MOS non-hard	ADI	2	2.0E-03			1994	>150			Sexton, 94IEEE Wrkshp Rec., pg 55.
ESA	**AD7893SQ**	**Serial 5.5 µs conv. time**	**LC^2MOS**	**ADI**	**14**	**~2.5E-05**			**1997**	**>68**		**CYC**	**Bee, et al, 98IEEE Wrkshp Rec., pg 58.**
JPL	ADC574A	Internal reference	CMOS/bipolar	BUB	<40				Jul-91	<<40			
JPL	ADC674	Internal reference	CMOS/bipolar	BUB	<40				Jul-91	<<40			
TRW	ADC85	Int. ref. Parallel & serial out		SIP					Jul-92	>60			T.C. Lunn
TRW	ADC87	Int. ref. Parallel & serial out		BUB					Jul-92		3.0E-05		T.C. Lunn. LU_{th} = ?. Cross section @ LET = 60.
LIN	ADS112	Internal reference, parallel out		DAT					Apr-91	38			
GSFC	**CS5012A**		**CMOS**	**CRY**	**3.5 to 4.8**				**Mar-97**	**11**			**LaBel, EEE Links, Vol. 3, No. 1, Mar 97**

Test Org.*	Device	Function	Technology	Mfr.	Effective SEU LET* Threshold	Device Xsection (cm^2)	Bits Tested	Bit Xsection (cm^2)	Test Date	LUth	LU Xsection (cm^2)	Fac.	Remarks 31-Aug-99
	Note: Entries in **RED** indicate data added since the 1997 Compendium.												
JPL/ HON	HI574	Internal reference	CMOS	HAR	10	8.0E-05			Dec-94	>120			D/C 9210
JPL	HI674ALD	Internal reference	DC9205	HAR	6	1.0E-04			Nov-92	>120			Tested to 80 °C. Earlier D/C (next entry) latches up.
JPL	HI674ASD	Internal reference	DC9028	HAR	6				Nov-92	30			See preceding entry.
JPL	HI774B	Internal reference, parallel out	BICMOS	HAR					Nov-92	<<60			D/C 9022. Also has latchups with ^{252}Cf.
GSFC	HS5212	Int. ref. Parallel & serial out	Hybrid	SIP	~1.4	1.0E-03			Feb-94	>80			LaBel, 1994 SEE Symposium.
HON	HS5214	Parallel and serial output	Bipolar hybrid	SIP	16	2.9E-05			Feb-93	>>37			Serial mode. Based on HS5212 data.
HON	HS5214 (AD5214)	Parallel and serial output		SIP	<11	1.5E-03			Feb-93	>37			D/C 9247. Parallel mode. Based on HS5212 data.
JPL	LTC1272	Parallel output	CMOS	LTN					Oct-92	<<30			
JPL	MN5253	Int. ref. Parallel & serial out	CMOS	MNC	16				Nov-89				Part bigger than beam.
JPL	MX674A	Internal reference	BiCMOS	MXM	~3	1.0E-03			Nov-92	>120			
JPL	MX7572	Internal reference, parallel out	Bipolar/CMOS?	MXM	20	2.0E-04			Nov-92	>120			
JPL	MX7672	Parallel and serial output	BiCMOS	MXM	20	2.0E-04			Nov-92	>120			
NSWC/ ARSP	RBC-12	Hard AD872	RBCMOS = RH BiCMOS	ADI	3	4.8E-03			1994	>126			Turflinger, 94IEEE TNS, No. 6, pg 2187. Noise cross section also exists.
NSWC/ ARSP	RBC-12	Flash. (hard AD872)	RBCMOS = RH BiCMOS	ADI	~10	1.0E-05			Apr-96	>126		UCB.	Turflinger, 94IEEE TNS, No. 6, pg 2187. Division by samples per irradiation recommended.
NSWC/ ARSP	RBC-12	Flash. (hard AD872)	RBCMOS = RH BiCMOS	ADI		5.0E-05			Apr-96	>126		UCB.	Turflinger, 94IEEE TNS, No. 6, pg 2187. Division by samples per irradiation recommended.
JPL	SP674AU/B	Internal reference	Some MOS	SIP					Mar-93	~26			Large variability. Some soft error data.
JPL	SP7800	Internal reference, parallel out	CMOS	SIP					Apr-92	<<30			
GSFC	SPT7922	Parallel output	Bipolar	SGP	<3.4	1.5E-03			1994	>120			LaBel. 94IEEE Wrkshp Rec., pg 64.
		ADC (14-bit)											
JPL	AD7872TQ	Serial Output	BiCMOS	ADI	~1.4	1.0E-03			Sep-92	>104			Slight differences in all "1s" and "0s".
JPL	**AD9240**	**10 MSPS Binary parallel output**	**CMOS**	**ADI**						**25**	**6.0E-04**	**TAM**	**Miyahira, preliminary JPL internal report.**
JPL	**AD9243**	**3 MSPS Binary parallel output**	**CMOS**	**ADI**						**25**	**6.0E-04**	**TAM**	**Miyahira, preliminary JPL internal report.**
JPL	**ADS-946-2**	**parallel output**	**CMOS**	**DAT**						**7.7**	**4.0E-06**	**TAM**	**Miyahira, preliminary JPL internal report.**
JPL	LTC1419		CMOS (epi?)	LTN	16	3.0E-05			Mar-97	>74		BNL	X-section @ LET = 40. Used 1 KHz sine wave input. Separate JPL report 6/97.
		ADC (16-bit)											
ESA	**AD676AD**	**Parallel, sucessive approx., 10 µs conv. Time**	**Hybrid Bi-MOS II**	**ADI**	**~1.8**	**>5.0E-04 dig. chip**			**1997**	**>28**		**CYC**	**Bee, et al, 98IEEE Wrkshp Rec., pg 58. Transient and lingering errors recorded.**
GSFC	AD676BD		Hybrid: CMOS & BiMOS II	ADI	<3.4				1994				

Test Org.*	Device	Function	Technology	Mfr.	Effective SEU LET* Threshold	Device Xsection (cm^2)	Bits Tested	Bit Xsection (cm^2)	Test Date	LUth	LU Xsection (cm^2)	Fac.	Remarks 31-Aug-99
	Note: Entries in **RED** indicate data added since the 1997 Compendium.												
Ball	AD677		Hybrid: CMOS & BiMOS II	ADI	3.4				Dec-94				
ESA	**AD7884AQ**	**Two pass flash, 5.3 s conv. Time**	**LC^2MOS**	**ADI**	**~2**	**2.5E-03**			**1997**	**>68**		**CYC**	**Bee, et al, 98IEEE Wrkshp Rec., pg 58.**
JPL	**AD9260**	**parallel, sigma-delta**	**CMOS**	**ADI**						**7.7**	**2.0E-05**	**TAM**	**Device failed after second latchup.**
GSFC	**AD976**	**parallel, internal 2.5V ref.**	**BiCMOS**	**ADI**	**<3.38**				**1997**	**>80**		**BNL**	**O'Bryan, et al, 98IEEE Wrkshp Rec., pg 39. D/C 9723**
JPL	ADS7805		CMOS/epi (7 µm.)	BUB					Dec-94				1.0E-5 @ LET = 15. Incomplete characterization.
GSFC	**ADS7805LPRP**	**100 KSPS. 100mW max. pwr dissapation. Parallel output**	**CMOS**	**SEI**	**<1.45**				**1997**	**~11.4**		**BNL**	**O'Bryan, et al, 98IEEE Wrkshp Rec., pg 39. D/C 9435. Latchup protection circuit test - OK.**
SEI	**ADS7809**	**100 KSPS. 100mW max. pwr dissapation. Serial output**	**CMOS**	**BUB**	**17.8**	**9.0E-05**			**Mar-97**	**19.4**	**3.0E-05**	**BNL**	**Layton, et al, 98IEEE Wrkshp Rec., pg 170. D/C 7550 & 9649**
SEI	**ADS7809**	**A/D(16-bit)**	**CMOS**	**BUB**	**18**	**5.0E-05**			**Mar-97**	**23**	**3.0E-05**	**BNL**	**Layton, P. J. Space Electronics Test Rept (3/27/97)**
SEI	**ADS7809LRP**	**100 KSPS. 100mW max. pwr dissapation. Serial output**	**CMOS**	**BUB**	**18**	**5.0E-05**			**Mar-97**	**19.9**	**3.0E-05**	**BNL**	**Layton, et al, 98IEEE Wrkshp Rec., pg 170.**
JPL	**ADS-937**	**parallel output, low power**	**CMOS (hybrid)**	**DAT**						**7.7**	**2.0E-04**	**TAM**	**Miyahira, preliminary JPL internal report. All upsets from gate array chip.**
JH/ S^3	CS5016		CMOS	CRY					Jan-91				
ARSP	CS5016		CMOS	CRY	10	1.0E-01			May-90				
ARSP	CS5016		CMOS/epi	CRY					May-91				
J/GDD	CS5327	Stereo	CMOS (analog & digital chips)	CRY	3	5.0E-03			Jul-93	9			
ARSP	HS9576RH		CMOS Hybrid	SIP	3	5.0E-04			Jan-92				
ARSP	MAX195		BiCMOS	MXM					1984				
		ADC (20-bit)											
JPL	**AD7714-3**	**24-bit (3.3 V)**	**CMOS/epi**	**ADI**					**Jun-97**	**55**	**2.0E-05**	**BNL**	**LU rate (GCR) = 1.5E-04/yr**
JPL	DDC101		CMOS/epi (9 to 11 µm epi)	BUB				TAM	Nov-95				
		Bus Controllers/Encoders											
GSFC	1XD3-0701	RS Encoder-Data Command	Rad Hard CMOS/epi	UTM	38	6.5E-04			1993	>120			LaBel, et al, 93IEEE Wrkshp Rec., pg 27.
JPL	AACS/IOU Custom	1553 Interface	CMOS/epi gate array	UTM	60	1.0E-05			Mar-93	>120			At 125°. C.
GSFC	Bus Controller	Bus	standard CMOS/epi	MHS	<11.5	1.5E-05			Jul-92	>87			LaBel. Fairchild-designed
GD	DDC61553	1553 Bus Controller	Hybrid CMOS	DDC									Latchup. See UTM UT1553.
JPL	HS15530RH	Manchester Encod/Decoder	CMOS	HAR	25	5.0E-05			May-88				
MMS	MA805	1553 Bus Controller	CMOS	MED					1992	<36	6.0E-05		Dufour, et al, 92IEEE Wrkshp Rec., pg 21.
GSFC	Serial Controller		standard CMOS/epi	MHS	4.5	4.0E-05			Jul-92	>87			

Test Org.*	Device	Function	Technology	Mfr.	Effective SEU LET* Threshold	Device Xsection (cm^2)	Bits Tested	Bit Xsection (cm^2)	Test Date	LUth	LU Xsection (cm^2)	Fac.	Remarks 31-Aug-99
	Note: Entries in **RED** indicate data added since the 1997 Compendium.												
MMS	ULA 5N104	ASIC (Bus)	Bipolar	FER	<5.5	2.0E-03			1992	>88			Dufour, et al, 92IEEE Wrkshp Rec., pg 21.
JPL	UT1553BCRTM	Bus Controller	CMOS/epi	UTM	60				May-91	>120			At 125°. C.
		DAC (8-bit)											
BREL	AD558		Bipolar-IIL	ADI	<<5	2.0E-04			Feb-92				
JPL	AD7225TQ		LCCMOS	ADI					Jan-97	>62		TAM	Nichols. 1961 MeV Xe at 45° C. Runs with PIC16674A microC.
MM	CA3338AD		CMOS/TTL	HAR	>119				May-93				
GSFC	DAC08AQ		Bipolar	PMI	~3.5	2.0E-02			Jul-94				
S^3	DAC8408		CMOS	PMI	45	4.0E-05			Jan-92				
GSFC	**DAC8800**	**Octal, serial input**		**ADI**	**>80**				**Apr-97**	**>80**			**LaBel, EEE Links, Vol. 3, No. 1, Mar 97, pg 5.**
		DAC (10-bit)											
JPL	AD7533		CMOS	ADI					Nov-92	>120			Tested up tp 125 °C.
JPL	MP7533		CMOS	MPS					Nov-92	>120			
		DAC (12-bit)											
JPL	AD562		Bipolar I	ADI	15	1.0E-06			Mar-86				
GSFC	AD565		Bipolar	ADI					Nov-94	>80			D/C 9145. LaBel.
BREL	AD7541ATQ/883B	Multiplying		ADI					May-93	>38.5			W. Will (WP-01). D/C 9139.
GD	AD7543			ADI		4.0E-06							
JPL	AD7545AKN	Multiplying with input latches	CMOS	ADI	>120				Apr-95	>120			Nichols. Tested to 80 °C. Only all "1s" tested.
ICI	**AD9713BSQ/883BUP**		**Advanced Oxide Isolated Bipolar**	**ADI**	**~1**	**1.5E-04**			**1997**	**>93**		**NCSL**	**Stapor, et al, Innovative Concepts Technical Paper. Rapid 20-80 mV shifts in output when clocked. D/C 9623.**
JPL	AM6012		Bipolar	AMD	15	1.0E-06			Mar-86				
ARSP	DAC8412		BiCMOS	PMI	25	2.0E-04			Oct-92				
JPL	HAR7574KN		CMOS	HAR					1995	>120			Nichols, et al, 95IEEE Wrkshp Rec., pg. 1. Tested up to 80 °C.
JPL	MP7545TD/883		CMOS	MPS	>120				Apr-95	>120			Nichols, et al, 95IEEE Wrkshp Rec., pg. 1. Tested up to 80 °C. Only all "1s" tested.
JPL	MP7645/TD883		CMOS	MPS	>120				Apr-95	>120			Nichols, et al, 95IEEE Wrkshp Rec., pg. 1. Tested up to 80 °C. Only all "1s" tested.
JPL	MX7545TQ		CMOS	MAX	>120				Apr-95	>120			Nichols, et al, 95IEEE Wrkshp Rec., pg. 1. Tested up to 80 °C. Only all "1s" tested.
JPL	MX7545TQ		CMOS	MAX	>120				Apr-95	>120		BNL	All '1s" only
GSFC	**MX7847TQ**	**Dual, parallel input**	**CMOS**	**MAX**	**~10**				**1997**	**>75**		**BNL**	**O'Bryan, et al, 98IEEE Wrkshp Rec., pg 39. D/C 9715**
HON	PM7545			PMI	24	1.4E-04			Oct-92	>>37			D/C 9142. WP-02.

Test Org.*	Device	Function	Technology	Mfr.	Effective SEU LET* Threshold	Device Xsection (cm^2)	Bits Tested	Bit Xsection (cm^2)	Test Date	LUth	LU Xsection (cm^2)	Fac.	Remarks 31-Aug-99
	Note: Entries in **RED** indicate data added since the 1997 Compendium.												
MMS	SOR7541	Multiplying	CMOS	SOR					1992	>116			Dufour, et al, 92IEEE Workshop Record, pg. 21.
		DAC (16-bit)											
MOT	AD1866			ADI	<<11	3.0E-05			Dec-94	>117			Preliminary data by Tet Pang. All "0s" worst case. 12 MSB tested. D/C 9320.
		DAC (18-bit)											
GSFC	**SP9380**			**SIP**	**1.45 to 3.4**				**1995**	**37 to 60**		**BNL**	**La Bel, et al, 96IEEE Wrkshp Rec., pg 19. Catastrophic Latchup.**
		DC/DC Power Converters											
GSFC	**7804**		**hybrid**	**ADA**	**>37**	**<1.0E-07**			**1997**			**BNL**	**O'Bryan, et al, 98IEEE Wrkshp Rec., pg 39.**
JPL	2680M-S05F	Single output, + 5 V	hybrid	MDI	6	2.0E-04			Aug-95	>60		BNL	Localized component error identified. SEUs were reset errors only
GSFC	2690R-D15F	Dual output, ± 15 V in.	hybrid	MDI	4 to 8	5.0E-04			Nov-94	>72			Reset errors
GSFC	5690R-D15	Dual output, ± 15 V in.	hybrid	MDI	>83				Mar-97			BNL	LaBel, EEE Links
GSFC	**5690R-D15**	**Dual output, + 15 V in.**	**hybrid**	**MDI**	**26.6**				**1996**			**BNL**	**LaBel, et al, 97IEEE Wrkshp Rec., pg14. SEB/SEGR @ LET = 30.7. Destructive condition @ LET = 52.6.**
GSFC	AHE2815D/HB	Dual output, ± 15 V in.	Bipolar	ADA	20	1.0E-04			Nov-94	27			D/C 9345. Destructive (SEGR?) power MOSFET switching "ON".
GSFC	AHE2815DF/CH-SLV	Dual output, ± 15 V in.	Bipolar	ADA	20	1.0E-04			Nov-94	27			D/C 9345. Destructive (SEGR?) power MOSFET switching "ON".
GSFC	**AHF2812**	**12V output**	**hybrid**	**ADA**	**<37 (dropouts)**				**1997**			**BNL**	**O'Bryan, et al, 98IEEE Wrkshp Rec., pg 39. ~10 ms dropouts. At LET = 26.6 dropouts @ 50% >< 83%**
JH	ART2815T & family	Triple output, ± 15 V in.	rad hard design [IC's etc]	ADA	>83				Feb-94	>83			Myers, et al, 94IEEE Wrkshp Rec., pg. 97.
GSFC	**ASA2805S/CH**	**Single output, + 5 V**	**hybrid**	**ADA**	**~14 (dropouts)**	**~4.0E-05**			**1997**		ADA	**BNL**	**O'Bryan, et al, 98IEEE Wrkshp Rec., pg 39. ~10 ms dropouts. At LET = 26.6 dropouts @ 0% load; <20% w/180 ohm int. resistor; 20>< 50% w/2K int. resistor.**
JPL	ATR2815D	Dual output, ± 15 V in.	rad hard design [IC's etc]	ADA	~24	1.0E-05			Dec-96	>44	1.0E-05	TAM	~13 ms dropout @ LET = ~24. X-section and permanent droput given @ LET = 44.
GSFC	**ATW2805S**	**Single output, + 5 V**	**hybrid**	**ADA**	**<37 (dropouts)**				**1997**			**BNL**	**O'Bryan, et al, 98IEEE Wrkshp Rec., pg 39. ~10 ms dropouts. At LET = 26.6 dropouts @ 70% >< 83%**
JPL	ATW2805S	Single output, + 5 V	CMOS (one IC)	ADA	~24	1.0E-05			Dec-96	>44		TAM	~8 ms dropout @ 24. X-section @ LET = 44. No permanent dropout at LET=44.
ARSP	ATW28XX		CMOS (one IC)	ADA					Oct-91	51 to 80			
GSFC	**ICL7662MTV-4**	**Voltage Converter**		**MAX**	**59.7**					**>80**		**BNL**	**LaBel, et al, 96IEEE Wrkshp Rec., pg 19. Data at Vcc = 15 - higher Vcc shows no errors.**
GSFC	**MCH2805S**	**Single output, + 5 V**	**hybrid**	**ITP**	**>100**							**BNL**	**LaBel, et al, 96IEEE Wrkshp Rec., pg 19. No SEEs @ LET = 100.**
GSFC	**MDI2680**	**DC/DC Power Converter**	**hybrid (proprietary mod)**	**MDI**	**30**							**BNL**	**LaBel, et al, 96IEEE Wrkshp Rec., pg 19. Drop-out required power cycling.**
GSFC	MDI2690R-D15F	Dual output, ± 15 V in.	hybrid	MDI	4 to 8	5.0E-04				>72		BNL	LaBel, et al, 95IEEE TNS, No. 6, pg. 1957. Reset errors only. No destructive condition.
GSFC	MFL2805S	Single output, + 5 V	hybrid	ITP					Nov-94	>72			No transient errors.
GSFC	MFL2812S	3-Output, + 5 V, ± 12 V	hybrid	ITP	50	5.0E-06			Nov-94	>72			Spikes are 0.6V, 5E-6 cm^2, < 20 nanosec.
GSFC	MFL2815D	Dual output, ± 15 V in.	hybrid	ITP	45 to 60				Nov-94	>72			

Test Org.*	Device	Function	Technology	Mfr.	Effective SEU LET* Threshold	Device Xsection (cm^2)	Bits Tested	Bit Xsection (cm^2)	Test Date	LUth	LU Xsection (cm^2)	Fac.	Remarks 31-Aug-99
	Note: Entries in **RED** indicate data added since the 1997 Compendium.												
GSFC	MFL2815S	Dual output, ± 15 V in.	hybrid	ITP					Nov-94	>72			No transient errors.
JPL	MHF2805D	Dual output, ± 5 V in.	hybrid	ITP					Jan-97			TAM	Nichols. No errors @ LET>94 [1961 MeV Xe @ 60°]. Input = 28V "on."
JPL	MHF2815D	Dual output, ± 15 V in.	hybrid	ITP					Jan-97			TAM	Nichols. No errors @ LET>94 [1961 MeV Xe @ 60°]. Input = 28V "on."
		DSP (16-bit)											
ARSP	320C25		CMOS	TIX					Sep-89	12	3.0E-03	UCB	
JPL/JH	320C25		CMOS/epi	TIX					May-91	27 to 36		BNL	JH: Lu_{th} = 27. JPL: Lu_{th} = 36; 26 @ 125 °C
JH	320C25		CMOS/epi (8 µm)	TIX					Apr-92	80		BNL	"New LU-proof" (~6 µm epi) may not be available.
CNES	320C25		CMOS/epi (15 µm)	TIX					Oct-89	14	1.0E-04	GANIL	D/C 8917.
CNES	320C25		CMOS/epi (15 µm)	TIX					Feb-90			IPN	Tandem could not locate LU_{th} because of insufficient range.
NRL	320C26			TIX						<<29.5	1.0E-02		Limited test for LU. Stapor memo for test of Feb 93.
JPL	ADSP1016A	Multiplier	CMOS	ADI						<<37	1.0E-04		
CNES	ADSP2100		CMOS/epi	ADI					Dec-89	<30	1.0E-04	GANIL	Matra Rept. Dec 89 & Dufour, et al, 92IEEE Wrkshp Rec., pg 21.
JH	ADSP2100		CMOS/epi (18 µm)	ADI						14		BNL	Commercial devices.
JH	ADSP2100		CMOS/epi (18 µm)	ADI								BNL	Same response as for previous entry.
JH	ADSP2100		CMOS	HTC					Apr-90	9		BNL	
JH	ADSP2100A		CMOS/epi (experimental)	ADI	13	5.0E-03				13.5		BNL	Kinnison, et. al., 91IEEE TNS, pg 1398. Some developmental (other epi thicknesses & well-depths) do not latchup.
MMS	ADSP2100A		CMOS/epi	ADI					1992	26	1.0E-03	GANIL	Dufour, et al, 92IEEE Wrkshp Rec., pg 21.
ESA	ADSP2100A		CMOS/epi (12.5 µm.) low power	ADI	~8		531	3.0E-06	Jun-92	12	2.0E-05	IPN	Harboe-Sorensen, 91IEEE TNS, pg 441.
ARSP	ADSP2100AGU		CMOS	ADI	7	~2.0E-04				10 to 18	3.0E-04	UCB	Koga, et. al., 96IEEE TNS, pg 2982. D/C 8950.
ARSP	ADSP2100ASG		CMOS	ADI					Feb-90	12	1.0E-03	UCB	
ARSP	ADSP2181ES & -KS		CMOS- 0.6 µm. feature	ADI	4	2.0E-04		1.0E-07 (mem)		4	~3.0E-03	UCB	Koga, et. al., 96IEEE TNS, pg 2982. D/C 9513. Memory only tested.
ARSP	PDSP16510A	FFT Processor	CMOS	PLS	3	1.0E-02				3	3.0E-04	UCB	Koga, et. al., 96IEEE TNS, pg 2982.
IBM	SM320E15			TIX					May-93			BNL	LU rates given for RAM and register. WP-02, Jim Pollock
ARSP	**SMJ320C50GFAM50**	**Fixed Point - SARAM**	**CMOS, 0.7µm feature, 6.5µm epi**	**TIX**	**3**	**1.0E-02**			**1997**	**>63**		**UCB**	**Crain, et al, 98IEEE Wrkshp Rec., pg 51. D/C 9711B. Lockup errors begin @ LET = 15.**
ARSP	**SMJ320C50GFAM50**	**Fixed Point - DARAM**	**CMOS, 0.7µm feature, 6.5µm epi**	**TIX**	**3**	**3.0E-03**			**1997**	**>63**		**UCB**	**Crain, et al, 98IEEE Wrkshp Rec., pg 51. D/C 9711B. Lockup errors begin @ LET = 15.**
ARSP	**SMJ320C50GFAM50**	**Fixed Point - PLU, ALU**	**CMOS, 0.7µm feature, 6.5µm epi**	**TIX**	**5**	**1.0E-03**			**1997**	**>63**		**UCB**	**Crain, et al, 98IEEE Wrkshp Rec., pg 51. D/C 9711B. Lockup errors begin @ LET = 15.**
ARSP	**SMJ320C50GFAM50**	**Fixed Point - NOP**	**CMOS, 0.7µm feature, 6.5µm epi**	**TIX**	**5**	**2.0E-04**			**1997**	**>63**		**UCB**	**Crain, et al, 98IEEE Wrkshp Rec., pg 51. D/C 9711B. Lockup errors begin @ LET = 15.**

Test Org.*	Device	Function	Technology	Mfr.	Effective SEU LET* Threshold	Device Xsection (cm^2)	Bits Tested	Bit Xsection (cm^2)	Test Date	LUth	LU Xsection (cm^2)	Fac.	Remarks 31-Aug-99
	Note: Entries in **RED** indicate data added since the 1997 Compendium.												
JH	TMC2310	FFT Processor	CMOS/epi	TRW					Jan-91	>>75		BNL	Kinnison
JPL	TMP320C50		CMOS/epi (prototype)	TIX					Jun-92	>69		BNL	Compare to TMS version below.
MMS	TMS320C25		CMOS	TIX	7	2.0E-02			1992	<37	2.0E-03	GANIL	Dufour, et al, 92IEEE Workshop, pg 21.
CNES	TMS320C25		CMOS/epi (15 µm)	TIX		2.0E-02			Jun-05	<<37	1.0E-04	GANIL	Adams, 91IEEE TNS, pg 1686.
JPL	TMS320C50		CMOS	TIX	3	5.0E-04			Aug-94	18	3.0E-4	BNL	Compare to TMP version above. SARAM partial Xsection
CNES	ZR34161		CMOS/epi (12 µm)	ZOR					Oct-89	~17	4.0E-03	GANIL IPN	Both tests showed same results.
		DSP (32-bit)											
CNES	96002	FPU	CMOS/bulk & 12 & 15 µm epi	MOT	1.7				1995	12	1.0E-01	IPN	Bezerra, RADECS 95, pg 296. Data slips also seen. 12µm version has reduced LU.
ARSP	320C30		CMOS/epi (7 µm.)	TIX	3	1.0E-04			Dec-92	10	2.0E-04	UCB	
CNES	ADSP21020	FPU		ADI	<4	5.0E-03		1.0E-06	1995	>12.7<<36	2.6E-02	IPN	Bezerra, RADECS 95, pg 296. SEUs mostly address errors.
ESA	**ADSP-21020KG-133**	**FPU**	**CMOS**	**ADI**	**7**	**2.0E-03**			**1996**	**29**	**9.0E-04**	**BNL**	**Harboe-Sorensen, et al, RADECS 97 Data Workshop, pg 97. D/C 9623, Rev 3 die.**
ESA	**ADSP-21020TG-120**	**FPU**	**CMOS**	**ADI**	**5**	**2.0E-03**			**1996**	**16.5**	**1.5E-02**	**BNL**	**Harboe-Sorensen, et al, RADECS 97 Data Workshop, pg 97. D/C 94269211/9502, Rev 1.**
ESA	**ADSP-21020TG-80**	**FPU**	**CMOS**	**ADI**	**5**	**2.0E-03**			**1996**	**12**	**3.0E-02**	**BNL**	**Harboe-Sorensen, et al, RADECS 97 Data Workshop, pg 97. D/C 9211/9528, Rev. 1.**
ARSP	DSP32C		CMOS	ATT	16	~3.0E-03				40 to 55	5.0E-06	UCB	Koga, et al, 96IEEE TNS, pg. 2982. D/C 9191.
ARSP	SMJ320C30GB		CMOS/epi (5 µm.); 0.8 µm feature	TIX	3	8.0E-04					5.0E-07	UCB	Koga, et al, 96IEEE TNS, pg 2982. X-section at Snapback(th)=~5. D/C 9543.
ARSP	**SMJ320C30GB**	**NOP, Cache, ALU**	**CMOS (V.5.3), 6.5 µm epi, 0.7 µm (min) feature size.**	**TIX**	**3**	**2.0E-04**			**1997**	**>63**		**UCB**	**Crain, et al, 98IEEE Wrkshp Rec., pg 51. D/C 9543. Snapback also observed.**
ARSP	**SMJ320C30GB**	**General Register**	**CMOS (V.5.3), 6.5 µm epi, 0.7 µm (min) feature size.**	**TIX**	**3**	**7.0E-04**			**1997**	**>63**		**UCB**	**Crain, et al, 98IEEE Wrkshp Rec., pg 51. D/C 9543. Snapback also observed.**
ARSP	**SMJ320C40HFM40**	**NOP**	**CMOS 50C21.22, 6.5 µm epi, 0.7 µm feature size**	**TIX**	**5**	**1.0E-05**			**1997**	**>63**		**UCB**	**Crain, et al, 98IEEE Wrkshp Rec., pg 51. D/C 9546A. Snapback also observed.**
ARSP	**SMJ320C40HFM40**	**Cache**	**CMOS 50C21.22, 6.5 µm epi, 0.7 µm feature size**	**TIX**	**3**	**3.0E-05**			**1997**	**>63**		**UCB**	**Crain, et al, 98IEEE Wrkshp Rec., pg 51. D/C 9546A. Snapback also observed.**
ARSP	**SMJ320C40HFM40**	**ALU**	**CMOS 50C21.22, 6.5 µm epi, 0.7 µm feature size**	**TIX**	**5**	**2.0E-05**			**1997**	**>63**		**UCB**	**Crain, et al, 98IEEE Wrkshp Rec., pg 51. D/C 9546A. Snapback also observed.**
ARSP	**SMJ320C40HFM40**	**General Register**	**CMOS 50C21.22, 6.5 µm epi, 0.7 µm feature size**	**TIX**	**5**	**7.0E-05**			**1997**	**>63**		**UCB**	**Crain, et al, 98IEEE Wrkshp Rec., pg 51. D/C 9546A. Snapback also observed.**
ARSP	**SMJ320C40HFM40**	**RAM**	**CMOS 50C21.22, 6.5 µm epi, 0.7 µm feature size**	**TIX**	**5**	**2.0E-03**			**1997**	**>63**		**UCB**	**Crain, et al, 98IEEE Wrkshp Rec., pg 51. D/C 9546A. Snapback also observed.**
ARSP	SMX320C30GB		CMOS/epi (6.5 µm.)	TIX	3	8.0E-04				10	3.0E-05	UCB	Koga, et al, 96IEEE TNS, pg 2982. D/C 9210.
ARSP	TMS320C30GB		CMOS/epi (13 µm.)	TIX	3	8.0E-04				10	3.0E-03	UCB	Koga, et al, 96IEEE TNS, pg 2982. D/C 9050.
ARSP	WE-DSP32C		CMOS	ATT					Jun-92	17	1.7E-02	UCB	

Heavy Ion SEE

Test Org.*	Device	Function	Technology	Mfr.	Effective SEU LET* Threshold	Device Xsection (cm^2)	Bits Tested	Bit Xsection (cm^2)	Test Date	LUth	LU Xsection (cm^2)	Fac.	Remarks 31-Aug-99
	Note: Entries in **RED** indicate data added since the 1997 Compendium.												
		DSP (56-bit)											
JH	DSP56001		CMOS	MOT					Jan-91	<27			
LIN	DSP56001		CMOS	MOT					Apr-91	12			For simple dynamic test.
		EDAC											
IBM	---	32-bit	CMOS	AMD	5	1.0E-04				25	5.0E-04	BNL	
MMS	54LS630	16-bit parallel	Bipolar-LSTTL	TIX	7	1.0E-04			1992	>32			
ARSP	54LS630	32-bit	Bipolar-LSTTL	TIX	7	1.0E-03				>32		GANIL	Dufour, et al, 92IEEE Wrkshp Rec., pg. 21.
MMS	54LS670	16-bit parallel	Bipolar-LSTTL	SGN	5	6.0E-04							
GSFC	54LS670	32-bit	Bipolar-LSTTL	SGN	5	6.0E-04	3700			>75		UCB	
ARSP	IDT49C460	32-bit	CMOS	IDT	17					25	2.0E-03	BNL	No SEU cross section @ LET=40 due to LU.
ARSP	IDT49C460	32-bit	CMOS	IDT	>100	1.0E-07			May-91	>100		UCB	
IBM	IDT49C460	32-bit	CMOS	IDT	15 to 20	5.0E-05			Nov-94	>80			LaBel. Cross section for all five error types monitored.
ARSP	IDT49C460	32-bit	CMOS	IDT	>100	1.0E-07			Jan-91	>100		UCB	
		Fiber Optics											
GDD	HFD3801-002	Fiber Optic Receiver	TTL Integrated	HON	~2	7.0E-02			Dec-90				LaBel, Operated as a pair with following entry. Proton data also exists.
GDD	HFE4811-013	Fiber Optic Transmitter	TTL Integrated	HON	13	3.0E-04			Dec-90				LaBel, Operated as a pair with preceding entry.
GDD	ODL200 REC	Fiber Optic Receiver (diode)	Bipolar/GaAlAs	ATT	~3	5.0E-04			Jan-94				LaBel, et al, 94IEEE Workshop Record, pg. 64.
GDD	ODL200TX	Fiber Optic Transceiver	Bipolar/GaAlAs	ATT	45 to 80				Jan-94				LaBel, et al, 94IEEE Workshop Record, pg. 64.
		FIFOs											
GSFC	7204	4K x 9	CMOS	IDT	8 to 11.6				Nov-94	16		BNL	LaBel. SEU cross section obscured by SEL.
JH	54AC708		CMOS/epi	NSC	21	8.0E-04			Jul-92			BNL	Kinnison 92IEEE Wrkshp Rec., pg 12. 10% of upsets are control errors.
MHS	67201F (Temic type)	512 x 9	CMOS	MHS			100			>100			TEMIC/Matra MHS Radiation Evaluation Results Table July,1996
MHS	67202F (Temic type)	1K x 9	CMOS	MHS	4		100			>100			TEMIC/Matra MHS Radiation Evaluation Results Table July,1996
MHS	67203E (Temic type)	2K x 9	CMOS	MHS	4		100			>100			TEMIC/Matra MHS Radiation Evaluation Results Table July,1996
MHS	67204E (Temic type)	4K x 9	CMOS	MHS	4		100			>100			TEMIC/Matra MHS Radiation Evaluation Results Table July,1996
GSFC	**6704EV-50**	**4K x 9**	**CMOS**	**MHS**	**see remarks**				**1997**			**BNL**	**O'Bryan, et al, 98IEEE Wrkshp Rec., pg 39. D/C 9636. LETth ~3 (byte errors): ~8 (control errors): ~35 (Mode Change)**
MHS	67205E (Temic type)	8K x 9	CMOS	MHS	4		100			>100			TEMIC/Matra MHS Radiation Evaluation Results Table July,1996

Test Org.*	Device	Function	Technology	Mfr.	Effective SEU LET* Threshold	Device Xsection (cm^2)	Bits Tested	Bit Xsection (cm^2)	Test Date	LUth	LU Xsection (cm^2)	Fac.	Remarks 31-Aug-99
	Note: Entries in **RED** indicate data added since the 1997 Compendium.												
JH	7134RT	8K x 8	CMOS	IDT					Apr-92			BNL	Kinnison 92IEEE Wrkshp Rec., pg 12. 10% of upsets are control errors.
ARSP	7201LA50TCB	512 x 9	CMOS	IDT					Sep-89	13	2.0E-03		
GSFC	7201T	512 x 9	CMOS- various split epi	IDT	<3.4				May-94	<26 to >80		BNL	LaBel, et al, RADECS 95, pg 258. Variable LU LETs from varied epi thicknesses (6, 8, 10 &12 µm). Only 6 µm epi devices did not latchup.
GSFC	7202RE	1K x 9	CMOS/epi (10 µm.)	IDT	3.5	4.2E-03		4.6E-07	Sep-92	38		BNL	LaBel
GSFC	7202RE	1K x 9	CMOS/epi	IDT					Sep-92	38		BNL	LaBel
JH	7202RT	1K x 9	CMOS	IDT					Apr-92	15		BNL	Kinnison
GSFC	7203ERP	2K x 9	CMOS	IDT	8 to 11.6				Nov-94	35		BNL	LaBel. SEU cross section obscured by SEL. Destructive bursts at LET = 20 (due to control areas?).
GSFC	7203L40DB	2K x 9	CMOS	IDT	3.4	5.5E-03			Jun-94	15 to 22		BNL	LaBel. D/C 3BC9334BP.
JH	74AC725		CMOS/epi	NSC	9	3.0E-03			1992			BNL	Kinnison 92IEEE Wrkshp Rec., pg 12. 10% of upsets are control errors. Possible "minilatch".
JPL	AM2813		PMOS	AMD	10	6.0E-03		2.0E-06				UCB	
JH/ NRL	AMD7202	1K x 9	CMOS	AMD					Jan-91	<26		BNL	
JH	AMD7204	4K x 9	CMOS	AMD					Jan-91	<26		BNL	
ARSP	C57401		CMOS	MMI					Jun-88	>60		UCB	
ARSP	CY7C401		CMOS	CYP					Jun-88	10	6.0E-04	UCB	
HON	CY7C429-30DM		CMOS	CYP	<<4.3				Apr-93	7.7		BNL	Pointer errors put device in an unknown state at LET = 6.4.
MMS	M67202	1K x 9	SCMOS/epi RT	MHS					1991	>140		GANIL	Dufour, et al, 92IEEE Wrkshp Rec., pg 21.
GSFC	**M67204EV-50**	**4K x 9**	**SCMOS/epi RT**	**MHS**	**37.1**				**1996**	**64.7**		**BNL**	**LaBel, et al, 97IEEE Wrkshp Rec., pg 14.**
ARSP	SSL7401		CMOS	SRT					Jun-88	>60		UCB	
		FPGAs											
JH	1020	2000 equiv. 2-input gates	CMOS/epi	ACT	25				Jan-91				Kinnison
HAR	3020	2000 equiv. 2-input gates	Rad Hard CMOS/SOI	HAR	100				May-93	>120			Harris Development Package
HAR	3090	9000 equiv. 2-input gates	Rad Hard CMOS/SOI	HAR	100				May-93	>120			Harris Development Package
SEI	**10009L**		**CMOS**	**GTF**					**Jan-97 Oct-96**	**7.7 to 12**	**3.0E-02**	**UCB TAM**	**Layton, et al, 98IEEE Wrkshp Rec., pg 170.**
MMS	1020 ??	2000 equiv. 2-input gates	CMOS/epi (1.2 µm. Feature)	ACT	24				Jul-93	0.76			Beaucour, 93IEEE Wrkshp Rec., pg 20.
CNES	1020A	2000 equiv. 2-input gates	CMOS/epi	TIX					Jan-92	>27			R. Ecoffet. D/C 9109. 547 logic modules, config. Antifuse.
CNES	1020A	2000 equiv. 2-input gates	CMOS/epi	TIX					Jan-92	>27			R. Ecoffet. D/C 9109. 547 logic modules, config. Antifuse.
JH	1020B	2000 equiv. 2-input gates	CMOS/epi	ACT	22								Kinnison. No latchup. Very similar to above.

Heavy Ion SEE

Test Org.*	Device	Function	Technology	Mfr.	Effective SEU LET* Threshold	Device Xsection (cm^2)	Bits Tested	Bit Xsection (cm^2)	Test Date	LUth	LU Xsection (cm^2)	Fac.	Remarks 31-Aug-99
	Note: Entries in **RED** indicate data added since the 1997 Compendium.												
JPL	1020B	2000 equiv. 2-input gates	CMOS/epi [TIX chip]	ACT					Dec-96 Nov-96	<<25	3.0E-05	TAM BNL	Swift: "TIX is very latchable."
GSFC	**3090A**	**9000 equiv. 2-input gates**	**CMOS**	**XIL**	**4 to 7**				**1996**	**4 to 7**		**BNL**	**LaBel, et al, EEE Links, Vol. 3, No. 1, Mar 97, pg 5 & 97IEEE Wrkshp Rec., pg14. Bit errors**
IBM	7256GC192-2	256 Flip-flops	CMOS	ALT					May-93				WP-2 (Jim Pollack). D/C 9249. Latchup rates given.
ARSP	A1010	1000 equiv. 2-input gates	CMOS/10 µm epi [2 µm feature]	ACT	25				Feb-90	>120			ACT I family; Feb 1990
ARSP	A1020	2000 equiv. 2-input gates	CMOS/10 µm epi [2 µm feature]	ACT	25				Feb-90	>120			ACT I family; Feb 1990
ARSP	A1020A	2000 equiv. 2-input gates	CMOS/epi [1.2 µm feature]	ACT	25				1994	>120			Koga, 94 SEE Symposium
ARSP	A1020B	2000 equiv. 2-input gates	CMOS/epi [1.0 µm feature]	ACT	~10	1.0E-03			1994	55	2.0E-05		Koga, 94 SEE Symposium. Matsushita dice. (for 200 F/Fs).
GSFC	A1020B	2000 equiv. 2-input gates	CMOS/epi [0.9 µm feature]	ACT	28		200			55		BNL	Katz, EEE Links, Nov., 96. "The only Actel device known to latchup."
JH	A1280	8000 equiv. 2-input gates	CMOS/epi (1.2 µm feature)	ACT	25	4.0E-05			Nov-93	>76			McKerracher (JH) & Katz (GSFC) - output latch/combinatorial logic
JH	A1280	8000 equiv. 2-input gates	CMOS/epi (1.2 µm feature)	ACT	5	4.0E-05			Nov-93	>76			McKerracher (JH) & Katz (GSFC) - output latch/sequential logic
ARSP	A1280	8000 equiv. 2-input gates	CMOS/epi (1.2 µm feature)	ACT	25				Dec-92	>120			Koga, 92IEEE TNS, No. 6, pg 1685. ACT II family. Combinatorial logic.
ARSP	A1280	8000 equiv. 2-input gates	CMOS/epi (1.2 µm feature)	ACT	5				Dec-92	>120			Koga, 92IEEE TNS, No. 6, pg 1685. ACT II family. Sequential logic.
ARSP/ GSFC	A1280A	8000 equiv. 2-input gates	CMOS/epi (1.0 µm feature)	ACT	28				1993	>100			Koga. ACT II. Combinatorial logic.
ARSP/ GSFC	A1280A	8000 equiv. 2-input gates	CMOS/epi (1.0 µm feature)	ACT	5				1993	>100			Koga. ACT II. Sequential logic.
ARSP/ GSFC	A1280A	8000 equiv. 2-input gates	CMOS/epi (1.0 µm feature)	ACT	28		200		1993	>100		UCB.	SEDR. C = combinatorial logic. ARSP: 1993, GSFC:11/96
ARSP/ GSFC	A1280A	8000 equiv. 2-input gates	CMOS/epi (1.0 µm feature)	ACT	5		800		1993	>100		UCB.	SEDR. S = sequential logic. ARSP: 1993, GSFC:11/96
ESA	A1280A	8000 equiv. 2-input gates	CMOS ACT2 [MAT chip] 1.0 µm	ACT	27	3.0E-06			Sep-96	>120		BNL	Mattsson, ESA Rept SE/REP/0047/K. C-modules - All "0s".
ESA	A1280A	8000 equiv. 2-input gates	CMOS ACT2 [MAT chip] 1.0 µm	ACT	10	1.5E-05			Sep-96	>120		BNL	Mattsson, ESA Rept SE/REP/0047/K. S-modules - All "1s".
ESA	A1280A	8000 equiv. 2-input gates	CMOS ACT2 [MAT chip] 1.0 µm	ACT	15	3.0E-06			Sep-96	>120		BNL	Mattsson, ESA Rept SE/REP/0047/K. I/O-module - All "1s".
GSFC	A1280A 3.6V	8000 equiv. 2-input gates	CMOS/epi (1.0 µm feature)	ACT								BNL	Katz, EEE Links, Nov 96. No LU. No SEDR.
GSFC	A1280XL	8000 equiv. 2-input gates	CMOS/epi [0.6 & 0.8 µm.]	ACT								BNL	Katz, EEE Links, Nov 96. No LU. SEDR.
SAAB	**A1280XL 3.3 V**	**8000 equiv. 2-input gates**	**CMOS (0.6 µm)**	**ACT**	**5**			**3.5E-06**	**1997**	**>110**		**CYC**	**Mattsson, et al, SAAB Doc. SE/REP/0078/K, 10/97. S-module. D/C 9709.**
SAAB	**A1280XL 3.3 V**	**8000 equiv. 2-input gates**	**CMOS (0.6 µm)**	**ACT**	**5**			**2.5E-06**	**1997**	**>110**		**CYC**	**Mattsson, et al, SAAB Doc. SE/REP/0078/K, 10/97. I/O-module. D/C 9709.**
SAAB	**A1280XL 3.3 V**	**8000 equiv. 2-input gates**	**CMOS (0.6 µm)**	**ACT**	**20**			**2.0E-06**	**1997**	**>110**		**CYC**	**Mattsson, et al, SAAB Doc. SE/REP/0078/K, 10/97. C-module. D/C 9709.**
SAAB	**A1280XL 5.0 V**	**8000 equiv. 2-input gates**	**CMOS (0.6 µm)**	**ACT**	**10**			**2.5E-07**	**1997**	**>110**		**CYC**	**Mattsson, et al, SAAB Doc. SE/REP/0078/K, 10/97. S-module. D/C 9709.**
SAAB	**A1280XL 5.0 V**	**8000 equiv. 2-input gates**	**CMOS (0.6 µm)**	**ACT**	**10**			**2.0E-07**	**1997**	**>110**		**CYC**	**Mattsson, et al, SAAB Doc. SE/REP/0078/K, 10/97. I/O-module. D/C 9709.**
SAAB	**A1280XL 5.0 V**	**8000 equiv. 2-input gates**	**CMOS (0.6 µm)**	**ACT**	**28**			**8.0E-07**	**1997**	**>110**		**CYC**	**Mattsson, et al, SAAB Doc. SE/REP/0078/K, 10/97. C-module. D/C 9709.**

Heavy Ion SEE

Test Org.*	Device	Function	Technology	Mfr.	Effective SEU LET* Threshold	Device Xsection (cm^2)	Bits Tested	Bit Xsection (cm^2)	Test Date	LUth	LU Xsection (cm^2)	Fac.	Remarks 31-Aug-99
	Note: Entries in **RED** indicate data added since the 1997 Compendium.												
GSFC	A14100A	10000 equiv. 2-input gates	CMOS/epi?	ACT	21		100					BNL	Katz, EEE Links, Nov 96. C-module. No LU. SEDR.
GSFC	A14100A	10000 equiv. 2-input gates	CMOS/epi?	ACT	8							BNL	Katz, EEE Links, Nov 96. S-module and I/O. No LU. SEDR.
GSFC	**A14100A**	**10000 equiv. 2-input gates**	**CMOS/epi?**	**ACT**	**8**				**1996**	**>80**		**BNL**	**LaBel, et al, 97IEEE Wrkshp Rec. , pg 14. S- & I/O-module errors.**
GSFC	**A14100A**	**10000 equiv. 2-input gates**	**CMOS/epi?**	**ACT**	**21**				**1996**	**>80**		**BNL**	**LaBel, et al, 97IEEE Wrkshp Rec. , pg 14. C-module errors.**
GSFC	A1460A	6000 equiv. 2-input gates	CMOS/epi (1.0 µm feature)	ACT	21		100	2.0E-07				BNL	Katz, EEE Links, p17, July 96. No LU. SEDR. Proton upsets for C-module.
GSFC	A1460A	6000 equiv. 2-input gates	CMOS/epi (1.0 µm feature)	ACT	8			1.0E-06				BNL	Katz, EEE Links, p17, July 96. No LU. SEDR. Proton upsets for S- & I/O-modules.
ESA	A1460A	6000 equiv. 2-input gates	CMOS ACT3 [MAT chip](0.8 µm]	ACT	32	3.0E-06		1.5E-06	Sep-96	>120		BNL	Mattsson, ESA Rept SE/REP/0047/K. Combinatorial logic - All "0s".
ESA	A1460A	6000 equiv. 2-input gates	CMOS ACT3 [MAT chip](0.8 µm]	ACT	8	1.5E-05		1.0E-05	Sep-96	>120		BNL	Mattsson, ESA Rept SE/REP/0047/K. Sequential logic - All "1s".
ESA	A1460A	6000 equiv. 2-input gates	CMOS ACT3 [MAT chip](0.8 µm]	ACT	10	2.0E-06		2.0E-06	Sep-96	>120		BNL	Mattsson, ESA Rept SE/REP/0047/K. I/O-module.
GSFC	**A1460A**	**6000 equiv. 2-input gates**	**CMOS/epi (1.0 µm feature)**	**ACT**	**6 - 8**				**1996**	**>80**		**BNL**	**LaBel, et al, 97IEEE Wrkshp Rec. , pg 14. S- & I/O-module errors.**
GSFC	**A1460A**	**6000 equiv. 2-input gates**	**CMOS/epi (1.0 µm feature)**	**ACT**	**25 - 30**				**1996**	**>80**		**BNL**	**LaBel, et al, 97IEEE Wrkshp Rec. , pg 14. C-module errors.**
GSFC	A1460A 3.3V	6000 equiv. 2-input gates	CMOS/epi (1.0 µm feature)	ACT	~25			8.0E-07				BNL	Katz, EEE Links, p17, July 96. C-module.
GSFC	A1460A 3.3V	6000 equiv. 2-input gates	CMOS/epi (1.0 µm feature)	ACT	<6			2.0E-06				BNL	Katz, EEE Links, p17, July 96. S-module.
ESA	A1460A 3.3V	6000 equiv. 2-input gates	CMOS ACT3 [MAT chip](0.8 µm]	ACT	20	6.0E-06		3.0E-06	Sep-96	>120		BNL	Mattsson, ESA Rept SE/REP/0047/K. Combinatorial logic - All "0s".
ESA	A1460A 3.3V	6000 equiv. 2-input gates	CMOS ACT3 [MAT chip](0.8 µm]	ACT	6	2.0E-05		2.0E-05	Sep-96	>120		BNL	Mattsson, ESA Rept SE/REP/0047/K. Sequential logic - All "1s".
ESA	A1460A 3.3V	6000 equiv. 2-input gates	CMOS ACT3 [MAT chip](0.8 µm]	ACT	8	7.0E-06		7.0E-06	Sep-96	>120		BNL	Mattsson, ESA Rept SE/REP/0047/K. I/O.
GSFC	**A32140DX**	**14000 gates**	**CMOS, 3200DX family**	**ACT**					**1997**	**>75**		**BNL**	**Katz, EEE Links, Vol. 3, No. 3, Sep 97, pg 16.**
SAAB	**A32140DX 3.3 V**	**14000 gates**	**CMOS, 3200DX family**	**ACT**	**5**			**3.0E-06**	**1997**	**>110**		**CYC**	**Mattsson, et al, SAAB Doc. SE/REP/0078/K, 10/97. S-module. D/C 9703.**
SAAB	**A32140DX 3.3 V**	**14000 gates**	**CMOS, 3200DX family**	**ACT**	**5**			**2.5E-06**	**1997**	**>110**		**CYC**	**Mattsson, et al, SAAB Doc. SE/REP/0078/K, 10/97. I/O-module. D/C 9703.**
SAAB	**A32140DX 3.3 V**	**14000 gates**	**CMOS, 3200DX family**	**ACT**	**15**			**2.0E-06**	**1997**	**>110**		**CYC**	**Mattsson, et al, SAAB Doc. SE/REP/0078/K, 10/97. C-module. D/C 9703.**
SAAB	**A32140DX 5.0 V**	**14000 gates**	**CMOS, 3200DX family**	**ACT**	**10**			**2.0E-06**	**1997**	**>110**		**CYC**	**Mattsson, et al, SAAB Doc. SE/REP/0078/K, 10/97. S-module. D/C 9703.**
SAAB	**A32140DX 5.0 V**	**14000 gates**	**CMOS, 3200DX family**	**ACT**	**2**			**2.0E-06**	**1997**	**>110**		**CYC**	**Mattsson, et al, SAAB Doc. SE/REP/0078/K, 10/97. I/O-module. D/C 9703.**
SAAB	**A32140DX 5.0 V**	**14000 gates**	**CMOS, 3200DX family**	**ACT**	**30**			**8.0E-07**	**1997**	**>110**		**CYC**	**Mattsson, et al, SAAB Doc. SE/REP/0078/K, 10/97. C-module. D/C 9703.**
GSFC	**A32200DX**	**20000 gates**	**CMOS, 3200DX family**	**ACT**					**1997**	**11**	**1.5E-05**	**BNL**	**Katz, EEE Links, Vol. 3, No. 3, Sep 97, pg 16. No saturation @ LET = 52.**
GSFC	AT6002-JC		CMOS/epi 0.8 µm feature	ATM	7 - 8				1996	11 to 11.4		BNL	Katz, EEE Links; LaBel, 96 IEEE Wrkshp Rec., pg 19.
GSFC	ATT2C04-2 ORCA	3500 -4300 equiv. Gates	CMOS 0.5 µm feature	ATT	<7.9					<7.9		BNL	Katz, EEE Links, p17, July 96 & LaBel, et al, 96IEEE Wrkshp Rec., pg 19. Configuration mode.
GSFC	ATT2C04-2 ORCA	3500 -4300 equiv. Gates	CMOS 0.5 µm feature	ATT	>10							BNL	Katz, EEE Links, p17, July 96 & LaBel, et al, 96IEEE Wrkshp Rec., pg 19. Data programmed in.

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Test Org.*	Device	Function	Technology	Mfr.	Effective SEU LET* Threshold	Device Xsection (cm^2)	Bits Tested	Bit Xsection (cm^2)	Test Date	LUth	LU Xsection (cm^2)	Fac.	Remarks 31-Aug-99
	Note: Entries in **RED** indicate data added since the 1997 Compendium.												
GSFC	**CLAy-31**	**RAM-based. 3134 equivalent Gates**	**GaAs.**	**NSC**	**5**					**>90**		**BNL**	**LaBel, et al, 97IEEE Workshop Rec., pg 14. Data errors.**
GSFC	**CLAy-31**	**RAM-based. 3134 equivalent Gates**	**GaAs.**	**NSC**	**11**					**>90**		**BNL**	**LaBel, et al, 97IEEE Wrkshp Rec. , pg 14. Reconfiguration/snapback errors.**
GSFC	CLAy-31	3134 equiv. Gates	RAM-based GaAs.	NSC	5			7.0E-08		>60		BNL?	Katz, EEE Links, Nov 96. SER = SEU in the configuration cell.
GSFC	CLAy-31	3134 equiv. Gates	RAM-based GaAs.	NSC	5			8.0E-07	1996	>90		BNL?	Katz, EEE Links, Nov 96. Data programmed in.
GSFC	CP20420	4245 equiv. 2-input gates	CMOS	CPT	~12.5				1994	>15 <27		BNL	LaBel, et al, 94IEEE Wrkshp Rec., pg 64.
GSFC	**KJ911**		**Rad-hard, 2 µm epi (3.0 V)**	**LMA**	**18.8**	**~1.5E-06**			**'96-'97**			**BNL**	**Katz, EEE Links, Vol. 3, No. 2, Jun 97, pg 24.**
GSFC	**MKJ911**		**CMOS, 10 µm epi (3.0 V)**	**MAT**	**13.2**	**3.0E-06**			**'96-'97**			**BNL**	**Katz, EEE Links, Vol. 3, No. 2, Jun 97, pg 24.**
GSFC	**MKJ911**		**CMOS, 10 µm epi (3.3 V)**	**MAT**	**18.8**	**~1.5E-06**			**'96-'97**			**BNL**	**Katz, EEE Links, Vol. 3, No. 2, , pg 24, Jun 97.**
GSFC	**QYH580 LPGA**	**35000 gates (3.3 V)**	**Bulk CMOS, 0.8 µm features**	**YAM**	**~37**	**2.0E-06**			**Feb-97**	**>70**		**BNL**	**Katz, et al, EEE Links, Vol. 3, No. 2, , pg 21, Jun 97.**
GSFC	**QYH580 LPGA**	**35000 gates (5.0 V)**	**Bulk CMOS, 0.8 µm features**	**YAM**	**~37**	**no sat.**			**Feb-97**	**~67**	**4.0E-05**	**BNL**	**Katz, et al, EEE Links, Vol. 3, No. 2, , pg 21, Jun 97. LU X-section @ LET = 78. LU @ 60 with 5.5 V.**
GSFC	RH1020	2000 equiv. 2-input gates	CMOS/epi [1.0 µm feature]	ACT								BNL	Katz, EEE Links, Nov 96. No LU. SEDR.
GSFC	RH1280	8000 equiv. 2-input gates	CMOS/epi [Rad Hard]	ACT	22			8.0E-06				BNL	Katz, EEE Links, Nov 96. No LU. SEDR . Proton upsets for C-module.
GSFC	RH1280	8000 equiv. 2-input gates	CMOS/epi [Rad Hard]	ACT	3			9.0E-06				BNL	Katz, EEE Links, Nov 96. No LU. SEDR . Proton upsets for S-module.
ESA	RH1280	8000 equiv. 2-input gates	CMOS/epi [Rad Hard Loral 0.8 µm]	ACT	27	1.7E-06		1.7E-06	Sep-96	>120		BNL	Mattsson, ESA Rept SE/REP/0047/K. C-module - All "0s".
ESA	RH1280	8000 equiv. 2-input gates	CMOS/epi [Rad Hard Loral 0.8 µm]	ACT	10	6.0E-06		6.0E-06	Sep-96	>120		BNL	Mattsson, ESA Rept SE/REP/0047/K. S-module - All "1s".
ESA	RH1280	8000 equiv. 2-input gates	CMOS/epi [Rad Hard Loral 0.8 µm]	ACT	15	1.0E-06		1.0E-06	Sep-96	>120		BNL	Mattsson, ESA Rept SE/REP/0047/K. I/O - All "1s".
GSFC	RH1280	8000 equiv. 2-input gates	CMOS 0.8 µm. feature	LFS	22			8.0E-06				BNL?	Katz, EEE Links, p 17, July 1996. C-module.
GSFC	RH1280	8000 equiv. 2-input gates	CMOS 0.8 µm. feature	LFS	3			9.0E-06				BNL?	Katz, EEE Links, p 17, July 1996. S-module.
ESA	RH1280 3.3V	8000 equiv. 2-input gates	CMOS/epi [Rad Hard Loral 0.8 µm]	ACT	15	4.0E-06		1.0E-06	Sep-96	>120		BNL	Mattsson, ESA Rept SE/REP/0047/K. C-module - All "0s".
ESA	RH1280 3.3V	8000 equiv. 2-input gates	CMOS/epi [Rad Hard Loral 0.8 µm]	ACT	6	1.0E-05		1.0E-05	Sep-96	>120		BNL	Mattsson, ESA Rept SE/REP/0047/K. S-module - All "1s".
ESA	RH1280 3.3V	8000 equiv. 2-input gates	CMOS/epi [Rad Hard Loral 0.8 µm]	ACT	10	2.0E-06		2.0E-06	Sep-96	>120		BNL	Mattsson, ESA Rept SE/REP/0047/K. I/O - All "1s".
SAAB	**RH1280 3.3 V**	**8000 equiv. 2-input gates**	**CMOS/epi [Rad Hard LMA 0.8 µm]**	**ACT**	**25**			**8.0E-07**	**1997**	**>110**		**CYC**	**Mattsson, et al, SAAB Doc. SE/REP/0078/K, 10/97. C-module. D/C 9617.**
SAAB	**RH1280 3.3 V**	**8000 equiv. 2-input gates**	**CMOS/epi [Rad Hard LMA 0.8 µm]**	**ACT**	**8**			**2.0E-06**	**1997**	**>110**		**CYC**	**Mattsson, et al, SAAB Doc. SE/REP/0078/K, 10/97. S- & I/O-modules. D/C 9617.**
SAAB	**RH1280 5.0 V**	**8000 equiv. 2-input gates**	**CMOS/epi [Rad Hard LMA 0.8 µm]**	**ACT**	**30**			**4.5E-07**	**1997**	**>110**		**CYC**	**Mattsson, et al, SAAB Doc. SE/REP/0078/K, 10/97. C-module. D/C 9617.**
SAAB	**RH1280 5.0 V**	**8000 equiv. 2-input gates**	**CMOS/epi [Rad Hard LMA 0.8 µm]**	**ACT**	**10**			**1.5E-07**	**1997**	**>110**		**CYC**	**Mattsson, et al, SAAB Doc. SE/REP/0078/K, 10/97. S- & I/O-modules. D/C 9617.**
MMS	TPC1020	2000 equiv. 2-input gates	CMOS/epi (1.2 µm feature)	TIX	20				Jul-93	>76			Beaucour, 93IEEE Wrkshp Rec., pg 20.
CNES	XC2064	1200 equiv. 2-input gates	CMOS/bulk	XIL	6	2.0E-02			1990	12.7	2.5E-04		Chapuis. Actel family.

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Test Org.*	Device	Function	Technology	Mfr.	Effective SEU LET* Threshold	Device Xsection (cm^2)	Bits Tested	Bit Xsection (cm^2)	Test Date	LUth	LU Xsection (cm^2)	Fac.	Remarks 31-Aug-99
	Note: Entries in **RED** indicate data added since the 1997 Compendium.												
CNES	XC3042	4200 equiv. 2-input gates	CMOS/bulk	XIL	6	3.0E-02			1990	<12.7	1.2E-03		Chapuis. Actel family.
ARSP/ GSFC	XC3090-70	9000 equiv. 2-input gates	CMOS/bulk	XIL					Jul-92	5	5.0E-03		DC9110 & 9045.
GSFC	XC3090A	9000 equiv. input gates	CMOS/bulk	XIL	4 - 7				1996	4 to 7		BNL	Katz, EEE Links, p 17, July, 1996 & LaBel, et al, 96 IEEE Wrkshp Rec., pg 19.
LMC	**XC4036XL**	**36K equiv. Gates**	**CMOS/7µm epi, 0.35µm feat. 3.3 V**	**XIL**	**<15**				**1997**	**>100**		**BNL**	**Lum, LMC Tech Memo TM26-98. 125° C. Upsets mainly in "basement" (control) logic.**
		Gate Arrays/PALs/PLAs											
SEI	**10050LPRP**	**50K Gate Reprogram. PLA**	**CMOS**		**11**	**3.7E-03**			**1997**	**>25**	**3.2E-03**	**BNL**	**Layton, et al, 98IEEE Wrkshp Rec., pg 170.**
ESA/ MMS	16L8	PLA	Bipolar IMPACT	TIX		1.3E-05			1993				H. Van Looy. ESA Rept. 1993
ESA	20RA10Z	Prog. Logic Device (PLD)	CMOS	SEQ		4.2E-05			Jun-91				Adams, ESA/ESTEC
IBM	22V10	PLA	CMOS	CYP	5	7.0E-06			1993	25	3.0E-04		Die sim ilar to below.
IBM	22V10	PLA	CMOS	MMI	5	1.0E-05			1993	25	3.0E-04		Die similar to above.
ESA/ MMS	22V10	PLA	Bipolar IMPACT	TIX		2.0E-05			1993				H. Van Looy. ESA Rept. 1993
GSFC	22V10B-15	PLA	CMOS	CYP					Dec-92	<<26			Compare above & below.
GSFC	22V10C-10	PLA	BiCMOS	CYP	>120				Dec-92	>120			Compare below.
GSFC	22V10D-15DMB	PLA	CMOS	CYP					Dec-92	<<26			Compare above & below.
SEI	**22V10FRP**	**Reprogrammable PLA**	**CMOS**		**<11**	**7.5E-05**			**1997**	**>80**		**BNL**	**Layton, et al, 98IEEE Wrkshp Rec., pg 170.**
SEI	**22V10RP**	**PLA**	**CMOS**		**<3**	**4.5E-04**			**1997**	**>117**		**BNL**	**Layton, et al, 98IEEE Wrkshp Rec., pg 170.**
GSFC	**22V10RPFE**	**PLA**	**CMOS**	**SEI**	**<3.38**				**1997**	**>72.9**		**BNL**	**O'Bryan, et al, 98IEEE Wrkshp Rec., pg 39. D/Cs XC34908493, XC34950484, 002611202. F/F errors.**
GSFC	**22V10RPFE**	**PLA**	**CMOS**	**SEI**	**~10**				**1997**	**>72.9**		**BNL**	**O'Bryan, et al, 98IEEE Wrkshp Rec., pg 39. D/Cs XC34908493, XC34950484, 002611202. Combinatorial errors.**
GSFC	AT22V10	PLA	CMOS	ATM	~10	3.0E-05			Aug-93	>80			LaBel, et al, 94IEEE Wrkshp Rec., pg 64.
IBM	BTVCMOS2	SPD3 Gate Array	CMOS II (Burlington, VT)	IBM	3				Jan-93	25			LU rates given by J. Pollock of WP-2. Tested by T. Scott
JPL	CDI6007	Gate Array	CMOS	LED	>75				Jun-85				
IBM	CY7C344	PLD	CMOS	CYP					Apr-93				D/C 9305 Latchup rates given. WP-2 (Jim Pollack)
ARSP	EP1210	PLD	CMOS (4 µm feature)	ALT					Jun-88	>100			String of D-type F/F's.
ARSP	EP1800	PLD	CMOS (2 µm feature)	ALT					Jun-88	15	2.0E-03		String of D-type F/F's.
McD	EP1810	Electronically PLD	CMOS bulk	ALT	<4	1.0E-02			Sep-93	5	1.0E-03		W. Zakrzewski, (Also tested EP610)
ESA	EP310	Prog. Logic Device (PLD)	C/NMOS?	ALT	5.4	3.6E-05			1991				Adams, ESA/ESTEC.
ROCK	EP310DM	UVE Electronically PLD	C/NMOS	ALT	12	1.8E-04							

Heavy Ion SEE

Test Org.*	Device	Function	Technology	Mfr.	Effective SEU LET* Threshold	Device Xsection (cm^2)	Bits Tested	Bit Xsection (cm^2)	Test Date	LUth	LU Xsection (cm^2)	Fac.	Remarks 31-Aug-99
	Note: Entries in **RED** indicate data added since the 1997 Compendium.												
ESA	EP600	PLD	C/NMOS?	ALT	8	3.0E-06			Jun-91				Adams, ESA/ESTEC. Fab from Intel wafers may change.
ROCK	EP600DM	UVE Electronically PLD	C/NMOS	ALT	12	1.8E-04							
BREL/ MCD	EP610	Electronically PLD	CMOS bulk	ALT					Oct-94	9	5.0E-04		Normand. D/C 9317, Temp = 44 to 100° C;
ARSP	EP910JC	UVE Electronically PLD	CMOS	ALT	4				Dec-89	15	7.0E-04		
PHY	EPM5032	UVE Electronically PLD	CMOS bulk	ALT					Mar-93	3	1.0E-03		Temp = 95° C. Rept. No. PHY-93R013
ARSP	HP03	Process Prog. GA	CMOS/epi	UTM	45				Dec-92	>80			Koga, 92IEEE-TNS, No. 6, pg 1685.
HON	HR1060	Gate Array	RICMOS III	HON	22				Jun-91	>120			Test Metal had 4 functions tested.
JPL	HR1060	Gate Array (custom CDU)	RICMOS III	HON	60				Mar-92	>120			Up to 125° C. Same fab, different implementation as preceding
GSFC	HR2340	Gate Array (multifunction)	RICMOS IV	HON									Soft latch?
GSFC	**HX2300**	**SOI Test Metal**	**RICMOS SOI 4**	**HON**	**>120**				**1995**	**>120**			**LaBel, et al, 96IEEE Wrkshp Rec., pg 19.**
GSFC	**IMP50E10**	**Electrically Programmable Analog Circcuit**	**CMOS**	**IMP**	**1.45**				**1995**	**15 to 26.6**			**LaBel, et al, 96IEEE Wrkshp Rec., pg 19.**
JPL	LCA10038Q	Process Prog. GA	HCMOS/epi (10 µm.)-- not RLSI	HON	30				Jul-93	>115			Only 64-bit RAM tested.
HAC	LCA200K Process	ASIC Process test chip	200K series ASIC process	LSI					Mar-93	5	4.0E-02		Shoga. LU=5 @ 37° & 3.2 @ 60° C. LU doesn't damage device.
GD/ARSP	LL7320Q	Process Prog. GA	CMOS	LSI	20				Dec-88	25	1.0E-04	Cf-252	
JPL/ARSP	LRH10038Q	Process Prog. GA	HCMOS/epi	LSI	30				Dec-88	>120			
LSI	LRH20K	PPGA Evaluation Device	Rad Hard HCMOS/epi	LSI	30	1.0E-06			Dec-92	>200			Owens, 92IEEE Wrkshp Rec., p 67. Config. as 1K SRAM.
ARSP	LRH91000	Process Prog. GA	CMOS/epi	LSI	50				Mar-90	>100			
ARSP	LRH9320Q	Process Prog. GA	Rad Hard HCMOS/epi	LSI	30				Dec-88	>120			Only 64-bit RAM tested
CNES	MB5000	Mem. Plan. GA	HCMOS/epi	MHS	30	5.0E-03			Nov-90				Chapuis. ESA Conf.
JPL	MB5000	Mem. Plan. GA	HCMOS/epi (10 µm)	MHS	40	5.0E-03			Aug-87				Tested as 256x7 RAM.
JPL	MB5000	Mem. Plan. GA	HCMOS/epi (8 µm)	MHS	25				Nov-87				Tested as 256x7 RAM.
MMS	MC Family	Gate Array	Rad Tol. 1 µm. SuperCMOS	MHS	32				Dec-90	>115			
MMS	MC5000	Gate Array 35K	SCMOS/epi RT	MHS					1992	>80			Dufour, et al, 92IEEE Wrkshp Rec., pg 21.
SOR	PAL16R8BMJ/883B	PLA	Bipolar (two parts)	AMD	7	2.5E-04			1993				J. Barak, 93IEEE Wrkshp Rec., pg 33. Test 8-bit reg. All "1s" worst case.
ARSP	PAL22V10A	PLA	Bipolar	AMD	4				Jun-92				
ARSP	PAL22V10A	PLA	Bipolar	TIX	4				Jun-92				
ARSP	PALC22V10B	PLA	CMOS	CYP	5				Dec-92	12	5.0E-04		

Test Org.*	Device	Function	Technology	Mfr.	Effective SEU LET* Threshold	Device Xsection (cm^2)	Bits Tested	Bit Xsection (cm^2)	Test Date	LUth	LU Xsection (cm^2)	Fac.	Remarks 31-Aug-99
	Note: Entries in **RED** indicate data added since the 1997 Compendium.												
ARSP	RA20K	Process Prog. GA	CMOS/epi	UTM	55				Mar-92	>120			Koga, et al, 92IEEE TNS, pg 1685. D-type F/F & SRAM.
IBM	RHCMOS2	Expressway GA	CMOS	IBM	>6				Jan-93	>120			T. Scott, IBM Letter
MMS	TIBPAL16R8	PLA	Bipolar	TIX	9				Jul-94	>140			Beaucour, 93IEEE Workshop, pg 20.
MMS	TIBPAL22V10	PLA	Bipolar	TIX	9				Jul-94	>140			Beaucour, 93IEEE Workshop, pg 20.
GSFC	UT22VP10	PLA or PAL	CMOS 1.2 µm feature. RADPAL	UTM	~60				Nov-96	>109		UCB	Amorphous Si based. Katz, EEE Links, summarizes Boeing data.
GSFC	UT22VP10	RADPAL	——	UTM	37					>90		BNL	LaBel, et al, 96IEEE Wrkshp Rec., pg 19.
UTM	UTD-R RA212	Gate Array	CMOS/epi (1.5µm feature)	UTM	55	7.0E-05							UTM says data apply to all UTD-R family
UTM	UTE-R 50K	Gate Array	CMOS/epi (5 µm)	UTM	~36				Jun-93	>165			
UTM	UTE-R 75K	Gate Array	CMOS/epi (3 metal overlayer)	UTM	0.36								Runaway in F/F support circuitry. D. Nichols observed P. Rudeck's test
JH		Gate Array	ECL. (1.0 & 1.5 µm feature sizes)	ASD	<1.4				Apr-90				1 & 1.5 µm feature sizes. 50 MHz.
JH		Gate Array as FIFO	rad-hard CMOS	UTM					Jul-92	>162			Kinnison, 92IEEE Wrkshp Rec., pg 12.
		Line Drvr/Rcvr/Xcvr											
LIN	26C31	Line driver	CMOS	NSC					1991	20			Sferrino '91
BREL	26C31	Line driver	CMOS	NSC					Jun-93				Latchup rate reported but no threshold. WP-01; Wes Will
LIN/S3	26C32	Line receiver	CMOS	NSC					1992	20			Sferrino '91; S(Cubed)='92
BREL	26C32	Line receiver	CMOS	NSC					1993				Latchup rate reported but no threshold. WP-01; Wes Will
JPL	32C278TM	Transceiver	CMOS	NSC					Dec-96	>152		TAM	Tested @ 25 °C.
GSFC	**54ABT245**	**Octal Transceiver**	**BiCMOS**	**NSC**	**>100**				**1997**	**>100**		**BNL**	**O'Bryan, et al, 98IEEE Wrkshp Rec., pg 39.**
GSFC	**54ABT245**	**Octal Transceiver**	**BiCMOS**	**PHL**	**>100**				**1997**	**>100**		**BNL**	**O'Bryan, et al, 98IEEE Wrkshp Rec., pg 39.**
ARSP	54AC245	Transceiver	ACMOS/no epi	FAS	60				Feb-90	70	2.0E-06	UCB	D/C 8747 11/88 & 8751 2/90.
ARSP	54AC245	Octal Transceiver	ACMOS/no epi	NSC	70	2.0E-06			Feb-90	60	2.0E-06		D/C 8747. *LU & SEU threshold are similar as given.
ARSP	54AC245	Transceiver	ACMOS/epi	NSC					1989	>120		UCB	
ARSP	54AC245	Transceiver	ACMOS/no epi	NSC					Feb-90	60		UCB	
JH	54ACTQ244	Octal buffer/driver	FACT w. I/O	NSC					Jan-91	>120			Based on similarity to 54ACTQ245 (below)
JH	54ACTQ244	Buffer/driver	FACT w. I/O	NSC					Jan-91	>120		BNL	
JPL	54ACTQ245	Octal Transceiver	FACT	NSC					Jan-91	>120			
JPL	54ACTQ245	Transceiver	FACT	NSC					Jan-94	>120		BNL	

Heavy Ion SEE

Test Org.*	Device	Function	Technology	Mfr.	Effective SEU LET* Threshold	Device Xsection (cm^2)	Bits Tested	Bit Xsection (cm^2)	Test Date	LUth	LU Xsection (cm^2)	Fac.	Remarks 31-Aug-99
	Note: Entries in **RED** indicate data added since the 1997 Compendium.												
ARSP	54ALS240	Octal buffer/driver	Bipolar-ALS-TTL	TIX					May-90				No latchup. May 90.
ARSP	54ALS241	Buffer	Bipolar-ALS-TTL	TIX					May-90				No latchup. May 90.
ARSP	54ALS244	Octal buffer/driver	Bipolar-ALS-TTL	TIX					May-90				No latchup. May 90.
JPL/ARSP	54HC244	Octal buffer/driver	HCMOS	TIX					Aug-88	>120			
JPL/ARSP	54HC245	Octal Transceiver	HCMOS	TIX					Dec-88	>120			
ARSP	54HCT240	Octal buffer/driver	HCMOS/TTL compatable	RCA						>80			Based on 54HCT244 data.
ARSP	54HCT244	Octal buffer/driver	HCMOS/TTL compatable	RCA						>80			
JPL/ARSP	54HCT244	Octal buffer/driver	HCMOS/TTL compatable	TIX						>168			D/C 8637. (4/87 & 5/87)
ARSP	54HCT245	Octal Transceiver	HCMOS/TTL compatable	RCA						>80			Based on 54HCT244 data.
GSFC	74FTC163245PV	Transceiver (3.3V/5V)	CEMOS (low power)	IDT					May-94	25	5.0E-04		Compare to IDT CEMOS register. LaBel
JPL	**74LVQ244**	**Buffer/epi (3.3 V)**	**CMOS**	**NSC**					**Apr-96**	**>120**		**BNL**	
GSFC	88C20	Diff Line receiver	CMOS	NSC	11	1.0E-05			Jan-94	>100			LaBel, 94 SEE Symposium
GSFC	88C30	Diff Line driver	CMOS	NSC	>120				Jan-94	>120			LaBel, 94 SEE Symposium
JPL	AD1485	Transceiver	CMOS	ADI					Dec-96	>90		TAM	Tested @ 88° C.
JPL	AD485AQ	Transceiver	CMOS	ADI					Dec-96	>152		TAM	Tested @ 90 °C.
GSFC	AD524	Diff amplifier	Bipolar	ADI	12	1.0E-03			Jun-94	>80			LaBel. DC 9344.
GSFC	AM7968 & AM7969	TAXI Transmitter & Receiver	Bipolar	AMD	<3.4				Jul-93	>53		BNL	LaBel, et al, 93IEEE Wrkshp Rec., pg 27.
GSFC	**AM7968 & AM7969**	**TAXI Transmitter & Receiver**	**Bipolar**	**AMD**	**<3.4**				**1996**	**>53**		**BNL**	**LaBel, et al, 97IEEE Wrkshp Rec., pg 14. Data and sync errors. Sync errors required several power resets.**
MMS	**AM79C98**	**Twisted Pair Transceiver**	**CMOS**	**AMD**	**>42**				**1995**	**50**	**5.0E-05**	**GANIL GSI**	**Poivey, et al, 96IEEE Wrkshp Rec. pg 73. D/C 9545. LU cross section @ LET=82.**
GSFC	AX3411	1553B Transceiver 15V	Bipolar	AFX	<11.5	3.0E-04			1994	>80			LaBel, et al, 94IEEE Wrkshp Rec., pg 64. D/C A67625.
GSFC	AX3453	1553B Transceiver 5V	Bipolar	AFX	<11.5	5.0E-05			1994	>80			LaBel, et al, 94IEEE Wrkshp Rec., pg 64.
GSFC	CT1487D	1553B Transceiver 15V	Bipolar	MED	11.5	5.5E-05			1994	>80			LaBel, et al, 94IEEE Wrkshp Rec., pg 64. D/C 9316.
GSFC	CT2521	1553B Transceiver 5V	Bipolar	MED	<26.5	4.5E-05			1994	>80			LaBel, et al, 94IEEE Wrkshp Rec., pg 64. D/C 9249. DUTs failed with Ni.
ESA	D469A	High Current Power Driver	CMOS/epi (PolyMOS)	SIL					1993	51	9.0E-05		H. Van Looy, ESA Rept.
GSFC	DDC63125 (ILC)	1553B Transceiver 15V	Bipolar	DDC	14	3.0E-04			1994	>80			LaBel, et al, 94IEEE Wrkshp Rec., pg 64.
MMS	**DP8392CV**	**Coaxial Transceiver Interface**	**Bipolar, Junc. Isol. Low Power Schottky**	**NSC**	**~1**	**2.0E-13**			**1995**	**>60**		**GANIL GSI**	**Poivey, et al, 96IEEE Wrkshp Rec., pg 73. D/C 9452. Transmit Mode. Errors normalized/transmitted bit.**
MMS	**DP8392CV**	**Coaxial Transceiver Interface**	**Bipolar, Junc. Isol. Low Power Schottky**	**NSC**	**~1**	**2.0E-14**			**1995**	**>60**		**GANIL GSI**	**Poivey, et al, 96IEEE Wrkshp Rec., pg 73. D/C 9452. Receive Mode. Errors normalized/transmitted bit.**

Test Org.*	Device	Function	Technology	Mfr.	Effective SEU LET* Threshold	Device Xsection (cm^2)	Bits Tested	Bit Xsection (cm^2)	Test Date	LUth	LU Xsection (cm^2)	Fac.	Remarks 31-Aug-99
	Note: Entries in **RED** indicate data added since the 1997 Compendium.												
BREL	DS26C32AMJ	Diff. Line receiver	CMOS/thick epi [mfr < 7/92] old	NSC						14	1.6E-04	UCB	Majewski, BREL Rept RTR-SLH-V1-A. Tested @ 5.25V& 100 °C.
BREL	DS26C32AMJ	Diff. Line receiver	CMOS/thin epi [mfr > 7/92] new	NSC					Mar-94	>77		UCB	Majewski, BREL Rept RTR-SLH-V2-A. Tested @ 5.25V& 100 °C.
GSFC	FC1553921	1553B Transceiver 5V	Bipolar	STC	<11.5	2.0E-03			1994	>80			LaBel, et al, 94IEEE Wrkshp Rec., pg 64. DUTs failed with Ni.
GSFC	Hot Rod REC	Transmitter/Receiver pair	GaAs	GAZ	<1.4	1.5E-03			1994	>120			LaBel, et al, 93IEEE Wrkshp Rec., pg. 27 & 94IEEE Wrkshp Rec., pg. 64. Proton data exist.
GSFC	Hot Rod TX	Transmitter/Receiver pair	GaAs	GAZ	<1.4	3.0E-03			1994	>120			LaBel, et al, 93IEEE Wrkshp Rec., pg. 27 & 94IEEE Wrkshp Rec., pg. 64. Proton data exist.
JPL GSFC	HS26C31	Diff. Line driver	HCMOS/SOS	HAR	>80				Sep-92	>120			LaBel, et al, 94IEEE Wrkshp Rec., pg 64. Tested up to 100° C.
JPL GSFC	HS26C32	Diff. Line receiver	HCMOS/SOS	HAR	>80				Sep-92	>120			LaBel, et al, 94IEEE Wrkshp Rec., pg 64. Tested up to 100° C.
GSFC	IDA07318	Laser Driver	Bipolar ECL	HPA					Aug-93	>80			LaBel Test Rept.
JPL	LTC1480	3.3V Transceiver	CMOS	LTN					Dec-96	>152		TAM	Tested @ 25 °C.
JPL	LTC1487	Transceiver	CMOS	LTN					Dec-96	<45	2.0E-07	TAM	
HON	LTC485	RS485 Transceiver	CMOS	LTN					Aug-93	14	1.3E-05		D/C 9227. WP2 (Jim Pollock)
ARSP	LTC485CN8	Transceiver	CMOS	LTN					Jun-91	3	8.0E-05		
JPL	**LV244**	**3V octal buffer driver**	**CMOS**	**PHL**					**Apr-96**	**>120**		**BNL**	**Tested @ 90 °C.**
JPL	**LVC245**	**3V octal bidirectional buffer**	**CMOS**	**PHL**					**Apr-96**	**85**		**BNL**	**Latchup current >50mA.**
GSFC	M63147	1553B Transceiver 5V	Bipolar	UTM	<11.5	1.0E-04			Aug-93	>80			LaBel, et al, 94IEEE Wrkshp Rec., pg 64.
JPL	MAX3485	3.3V Transceiver	CMOS	MAX					Dec-96	>152		TAM	No LU with LET = 152 @ 25 °C.: SEL at LET = 152 @ 90 °C.
JPL	MAX485E	Transceiver	CMOS	MAX					Dec-96	>152		TAM	Tested @ 25 °C.
ARSP	MC10H115	Receiver	Bipolar- ECL	MOT					Feb-90	>100			
JPL	MIC4420	Buffer driver	CMOS	MIC					Aug-92	>120			Includes temp up to 125° C
GSFC	MIC4427	MOSFET driver	4426/4427/4428 family	MIC						>90		BNL	Skipper, 95IEEE Wrkshp Rec., pg 50. p+ isolations prevent LU.
HON	MIC4428	MOSFET driver	CMOS	MIC					Oct-92	>37			Martinez. D/C 9234. Tested @ 120° C. No transients @ 12 V.
GSFC	**MIC4429AJB**	**Linear Driver**	**CMOS**	**MIC**	**>84.7**				**1997**	**>84.7**		**BNL**	**O'Bryan, et al, 98IEEE Wrkshp Rec., pg 39. No memory elements.**
GSFC	NH1500	1553B Transceiver 15V	Bipolar-- National Hybrids	NSC	<11.5	6.0E-06			Aug-93	>80			LaBel, et al, 94IEEE Wrkshp Rec., pg 64. D/C 9328. Die bigger than beam.
GSFC	NH1529	1553B Transceiver 5V	Bipolar-- National Hybrids	NSC	<11.5	1.5E-05			Aug-93	>80			LaBel, et al, 94IEEE Wrkshp Rec., pg 64. D/C 9329.
JH	P54PCT245	Octal transceiver, 3-state	CMOS	PFS					1989	<40			
LIN	P54PCT245	Octal transceiver, 3-state	CMOS	PFS					Apr-91	<27			

Test Org.*	Device	Function	Technology	Mfr.	Effective SEU LET* Threshold	Device Xsection (cm^2)	Bits Tested	Bit Xsection (cm^2)	Test Date	LUth	LU Xsection (cm^2)	Fac.	Remarks 31-Aug-99
	Note: Entries in **RED** indicate data added since the 1997 Compendium.												
JPL	SA3297	Periph.-Bus Transceiver	CMOS/bulk Twin Well	SNL	>120				Oct-88	>120		BNL	Similar to 54LS245.
JPL	SN75LBC176	Transceiver	CMOS	TIX					Dec-96	90		TAM	SEL at LET=90 @ 88° C.
GSFC	**SNJ54ABT245AJ**	**Octal buffer driver**	**CMOS**	**TIX**	**>100**				**1997**	**>100**		**BNL**	**O'Bryan, et al, 98IEEE Wrkshp Rec., pg 39.**
JPL	SP485ES	Transceiver	CMOS	SIP					Dec-96	>152		TAM	No LU with LET = 152 @ 25 °C.: SEL at LET = 152 @ 90 °C.
GSFC	TAXI	Transmitter/Receiver pair	Bipolar	AMD					1993	>50			LaBel, et al, 93IEEE Wrkshp Rec., pg 27.
JPL	TC4428	MOSFET driver	CMOS	TCS					Dec-96	~24	1.0E-06	TAM	Easy burnout.
JH	TSC430	FET Driver	CMOS/epi	TEL					Jan-91	>120			
GSFC	TSC4429	MOSFET driver		TEL	>120				Jan-94	>120			LaBel, et al, 94IEEE Wrkshp Rec., pg 64.
GSFC	UT63M125	1553B Transceiver 15V	Bipolar	UTM	<11.5	3.0E-04			1994	>80			LaBel, et al, 94IEEE Wrkshp Rec., pg 64. D/Cs 9250/9315.
GSFC	UT63M125	1553 bus transceiver	Bipolar	UTM	11				Jun-93	27			M. Gates. One maverick LU at LET=11.
GSFC	**UT63M147-BPC**	**1553 Tranceiver**	**CMOS**	**UTM**	**11**				**1996**	**>35**		**BNL**	**LaBel, et al, 97IEEE Wrkshp Rec., pg 14.**
		Logic Devices											
BREL	555	Timer	Bipolar	NSC	5	2.0E-05			Feb-92				
BREL	555	Timer	Bipolar	SGN	5	2.0E-05			Feb-92				
JPL	7495	Shift Register	Bipolar-TTL	TIX	~75				May-81				SEU response expected to be the same as that of 5495
JPL	54109	Dual JK-type F/F	Bipolar-TTL	SGN	>75							UCB	
JPL	54161	4-Bit Counter	Bipolar-TTL	RAY	>75							UCB	
JPL	74162	4-Bit Counter	Bipolar-TTL	FAS	>75							UCB	
GD/ARSP	25HCT04	Logic (SAR)	HCMOS/TTL compat.	ZYR					Jul-91	22	3.0E-04		GD: LU with Cf-252
ARSP	25LS 07	D-type F/F	Bipolar-LSTTL	AMD	13	3.0E-04	5000					UCB	
JPL	25LS374	Octal D-type F/F	Bipolar-LSTTL	AMD	8	5.0E-05	600					UCB	
JPL	54 73	4-bit JK-type F/F	Bipolar-TTL	SGN	>75							UCB	
JPL	54 95	Shift Register	Bipolar-TTL	SGN	>75							UCB	
JPL	54169 (SA3269)	4-Bit Counter	CMOS (80 Kohm)	SNL	>55								Development Part.
JPL	54395 (SA3270)	Shift Register	CMOS (80 Kohm)	SNL	>55								Development Part.
JH	54AC 02	Quad NOR gate	FACT	NSC					1990	>75		BNL	Kinnison. No LU at room T at LET=75.
JH	54AC 08	Quad 2-input AND Gate	FACT	NSC					1990	>75		BNL	Kinnison. No LU at room T at LET=75.

Test Org.*	Device	Function	Technology	Mfr.	Effective SEU LET* Threshold	Device Xsection (cm^2)	Bits Tested	Bit Xsection (cm^2)	Test Date	LUth	LU Xsection (cm^2)	Fac.	Remarks 31-Aug-99
	Note: Entries in **RED** indicate data added since the 1997 Compendium.												
CNES	54AC 74	Dual D-type F/F	AdvCMOS/epi	NSC					Feb-90	>75		IPN	Kinnison. No LU at room T at LET=75.
ARSP	54AC138	3 to 8 line decoder	ACMOS/no epi	FAS	70	2.0E-06			Nov-88	70	2.0E-06	UCB	LU & SEU threshold are similar as given. D/C 8627.
ARSP	54AC138	3 to 8 line decoder	ACMOS/epi	NSC					Dec-88	>100		UCB	No LU at 20 °C.
ARSP	54AC138	3 to 8 line decoder	ACMOS/bulk	NSC					Dec-88	25	4.0E+01	UCB	
ARSP	54AC163	Binary Counter	ACMOS/bulk	FAS	40	1.0E-05			Feb-90	40	1.0E-05	UCB	LU & SEU threshold are similar as given. D/C 8718.
ARSP	54AC163	Binary Counter	ACMOS/epi	NSC	40	2.0E-05			Dec-89	>120			D/C 8909
ARSP	54AC163	Binary Counter	ACMOS	NSC					Feb-90	>100	4.0E+01	UCB	Compare to GANIL data of adjacent parts.
CNES	54AC163	Binary Counter	ACMOS	NSC					Feb-90	>80	4.0E+01	GANIL	Compare GANIL data with adjacent parts.
ARSP	54AC174	Hex D-F/F	AC/epi	NSC	55	3.0E-05			Dec-89	>120			D/C 8922
JH	54AC174	Hex D-F/F	FACT*	NSC					1989			BNL	FACT for D/C later than 8826 are designed to be LU-proof.
ARSP	54AC299	Storage Register	ACMOS/no epi	FAS	60	2.0E-05			Feb-90	60	2.0E-05	UCB	LU & SEU threshold are similar as given. D/C 8741.
ARSP	54AC299	Storage Register	ACMOS/epi	NSC	50	3.0E-05			Dec-89	>120		UCB	D/C 8922
ARSP	54AC299	Storage Register	ACMOS/no epi	NSC					Feb-90	60		UCB	
JPL	54AC373	Octal 3-state transparent latch	ACMOS/no epi	FAS					Aug-87	<40	4.0E+01	UCB	
ARSP	54AC374	Octal D-type F/F	ACMOS/no epi	FAS	70	2.0E-06			Nov-88	70	2.0E-06	UCB	LU & SEU threshold are similar as given. D/C 8638.
ARSP	54AC374	Octal D-type F/F	ACMOS/epi	NSC	~50	2.0E-06			Nov-88	>120		UCB	D/C 8840
ARSP	54AC374	Octal D-type F/F	ACMOS/epi	NSC					Dec-88	>80		UCB	
MMS	54ACT163	Binary Counter	FACT	MHS	80	6.0E-06			1992	>140		GANIL	Dufour, et al, 92IEEE Wrkshp Rec., pg 21.
JH	54ACT163	Binary Counter	FACT*	NSC					1989	>75		BNL	FACT for D/C > 8826 are designed to be LU-proof
CNES	54ACT163	Binary Counter	ACMOS/T	RCA					Oct-89	<37		GANIL	
ARSP	54ACT174	Hex D-type F/F	ACT/epi	NSC	60	9.0E-05			Aug-89	>120		UCB	D/C 8920
ARSP	54ACT373	Octal 3-state transparent latch	FACT[ACT/epi]	NSC	40	2.0E-04			Dec-89	>120		UCB	D/C 8948
ARSP	54ACT374	Octal D-type F/F	ACMOS/T-no epi	FAS	60	5.0E-06			Feb-90	60	5.0E-06	UCB	D/C 8745. LU & SEU threshold are similar as given. Compare JPL data.
JPL	54ACT374	Octal D-type F/F	ACMOS/T-no epi	FAS					Aug-87		4.0E+01	UCB	
MMS	54ACT374	Octal D-type F/F	FACT	MHS	>140				1992	>140			Dufour, et al, 92IEEE Wrkshp Rec., pg 21.
ARSP	54ACT374	Octal D-type F/F	ACMOS/T	TIX					Feb-90	50		UCB	
HON	54ACTQ373	Octal 3-state transparent latch	ACTQ/?	NSC	29	8.6E-05			Oct-92	>>37		BNL	D/C Q9068942 WP-02

Test Org.*	Device	Function	Technology	Mfr.	Effective SEU LET* Threshold	Device Xsection (cm^2)	Bits Tested	Bit Xsection (cm^2)	Test Date	LUth	LU Xsection (cm^2)	Fac.	Remarks 31-Aug-99
	Note: Entries in **RED** indicate data added since the 1997 Compendium.												
ARSP	54AHCT109	Dual JK-type F/F	Adv. HCMOS	ZTX	60	1.0E-06				>37			
ARSP	54AHCT373	Octal 3-state transparent latch	Adv. HCMOS	ZTX	28	2.0E-05							
ARSP	54AHCT374	Octal D-type F/F	Adv. HCMOS	ZTX	28	4.0E-05							
ARSP	54ALS 74	Dual D-type F/F	Bipolar-ALS-TTL	TIX	5	1.5E-04	7500					UCB	
ARSP	54ALS112A	Dual JK-type F/F	Bipolar-ALS-TTL	TIX	7	1.0E-04	5000					UCB	
ARSP	54ALS175	Quad D-type F/F	Bipolar-ALS-TTL	TIX	8	1.0E-04	2500					UCB	
ARSP	54ALS240	Buffer	Bipolar-ALS-TTL	TIX					May-90			UCB	No latchup.
ARSP	54ALS241	Buffer	Bipolar-ALS-TTL	TIX					May-90			UCB	No latchup.
ARSP	54ALS244	Buffer	Bipolar-ALS-TTL	TIX					May-90			UCB	No latchup.
ARSP	54ALS273	Octal D-type F/F	Bipolar-ALS-TTL	TIX	4	5.0E-04	6300					UCB	
ARSP	54ALS373	Octal 3-state transparent latch	Bipolar-ALS-TTL	TIX	8	5.0E-05	8	6.3E-06				UCB	See following two entries-- nonagreement.
JPL	54ALS373	Octal 3-state transparent latch	Bipolar-ALS-TTL	TIX	8	4.5E-04	8	5.6E-05	Dec-86			BNL	See above.
JPL	54ALS373	Octal 3-state transparent latch	Bipolar-ALS-TTL	TIX	4	4.0E-04	8	5.0E-05	Feb-89			UCB	See above.
ARSP	54ALS374	Octal D-type F/F	Bipolar-ALS-TTL	TIX	5	3.0E-04	8	3.8E-05	Dec-87				Buchner, et al, 87IEEE-TNS, No. 6, pg 1232 reports LET = 3
ARSP	54AS109	Dual JK-type F/F	Bipolar-AS-TTL	TIX	6	8.0E-05		4.0E-05				UCB	
ARSP	54AS374	Octal D-type F/F	Bipolar-AS-TTL	TIX	7	3.0E-04		4.0E-05				UCB	
ARSP	54AS533	D-Latch	Bipolar-AS-TTL	TIX	28	3.0E-05		4.0E-06				UCB	
HON	54BCT373W	Octal Latch	BCT	TIX	>37				Oct-92	>37			
ARSP	54F 74	Dual D-type F/F	Bipolar-FTTL	SGN	8	1.0E-04		5.0E-05	Feb-89			UCB	
ARSP	54F109	Dual JK-type F/F	Bipolar-FTTL	FAS	11	2.0E-05		5.0E-05				BNL	
ARSP	54F373	Octal 3-state transparent latch	Bipolar-FTTL	FAS	25	2.0E-05		2.5E-06	Dec-86			BNL	
ARSP	54F373	Octal 3-state transparent latch	Bipolar-FTTL	FAS	15 & 25	2.0E-04		2.5E-06	Nov-89			UCB	Two parts @ each LET.
ARSP	54F374	Octal D-type F/F	Bipolar-FTTL	FAS	8	5.0E-05		6.3E-06				BNL	
ARSP	54FCT374	Octal D-type F/F	CMOS	IDT	55	4.0E-06			Feb-89	>100		UCB	
JPL	54HC 00	Quad NAND gate	HCMOS	STM					Aug-88	>120			
JPL	54HC 00	Quad NAND gate	HCMOS	TIX					Aug-88	>120			
ARSP	54HC 02	Quad NOR gate	HCMOS	RCA					Mar-88	>80			

Test Org.*	Device	Function	Technology	Mfr.	Effective SEU LET* Threshold	Device Xsection (cm^2)	Bits Tested	Bit Xsection (cm^2)	Test Date	LUth	LU Xsection (cm^2)	Fac.	Remarks 31-Aug-99
	Note: Entries in **RED** indicate data added since the 1997 Compendium.												
JPL	54HC 02	Quad NOR gate	HCMOS	TIX					Aug-88	>60			
ARSP	54HC 03J	Quad 2-input NAND gate	HCMOS	TIX					Aug-88	>120			
ARSP	54HC 04	HEX Inverter	HCMOS	NSC					Mar-88	>60		UCB	
JPL	54HC 04	HEX Inverter	HCMOS	TIX					Aug-88	>180			
JPL	54HC 08	Quad 2-input AND Gate	HCMOS	TIX					Aug-88	>120			
JPL/ARSP	54HC 11	Triple 3-input AND gates	HCMOS	TIX					Aug-88				
JPL	54HC 20	Triple 4-input NAND gate	HCMOS	TIX					Aug-88				
JPL	54HC 73	4-bit JK-type F/F	HCMOS	NSC	>75					>75		UCB.	
ARSP	54HC 73	4-bit JK-type F/F	HCMOS	RCA					Jun-88	>100		UCB.	
JPL	54HC 74	Dual D-type F/F	HCMOS	TIX					Aug-88	>80			
JPL/ARSP	54HC 85	4-bit magnitude comparator	HCMOS	TIX					Aug-88	>120			
JPL	54HC 86	Quad 2-input OR gate	HCMOS	TIX					Aug-88	>100			
ARSP	54HC109	Dual JK-type F/F	HCMOS	MOT	>75					>80		UCB.	
JPL	54HC109	Dual JK-type F/F	HCMOS	TIX					Aug-88	>120		UCB.	
ARSP	54HC109	Dual JK-type F/F	HCMOS	TIX	100		2		Mar-90			UCB.	
JPL	54HC125	Quad 3-state buffer	HCMOS	TIX					Aug-88	>60			
JPL	54HC138	3 to 8 line decoder	HCMOS	STM					Aug-88	>120			
JPL/ARSP	54HC138	3 to 8 line decoder	HCMOS	TIX					Aug-88	55			
JPL	54HC139	Dual decoder/deMUX	HCMOS	TIX					Aug-88	>80			
ARSP	54HC147	10 to 4 line priority decoder	HCMOS	TIX						>120			
ARSP	54HC151	8 to 1 multiplier	HCMOS	NSC					Mar-88	>60		UCB	
JPL	54HC151	8 to 1 multiplier	HCMOS	TIX					Dec-88	>120			
ARSP	54HC154	4 to 16 line Decoder/deMUX	HCMOS	RCA					Mar-88	>120			
JPL	54HC154	4 to 16 line Decoder/deMUX	HCMOS	TIX					Dec-88	>60			
JPL	54HC157	4 to 16 Decoder/MUX	HCMOS	TIX					Dec-88	>80			
ARSP	54HC160	Presettable decade counter	HCMOS	TIX						>120			
JPL	54HC161	4-bit presettable counter	HCMOS	TIX					Dec-88	>120			Tested to 60 °C. Later vintage than following

Test Org.*	Device	Function	Technology	Mfr.	Effective SEU LET* Threshold	Device Xsection (cm^2)	Bits Tested	Bit Xsection (cm^2)	Test Date	LUth	LU Xsection (cm^2)	Fac.	Remarks 31-Aug-99
	Note: Entries in **RED** indicate data added since the 1997 Compendium.												
HAC/ARSP	54HC161	4-bit presettable counter	HCMOS	TIX						33	4.0E-06		Latchup. Earlier vintage than preceding entry.
ARSP	54HC164	8-bit Ser/Par shift register	HCMOS	TIX	40	4.0E-05			Mar-90	>75			
ARSP	54HC165	8-bit Par/Ser shift register	HCMOS	RCA					Mar-88	>60			
JPL	54HC165	8-bit Par/Ser shift register	HCMOS	TIX					Dec-88	>12			Tested to 60 °C. Later vintage than following
ARSP	54HC165	8-bit Par/Ser shift register	HCMOS	TIX	40		8			55			Earlier vintage than preceding.
ARSP	54HC166	8-bit shift register	HCMOS	TIX						>120			
JPL	54HC174	Hex D-type F/F	HCMOS	STM					Aug-88				
ARSP	54HC174	Hex D-type F/F	HCMOS	TIX					Aug-88	>120			
JPL	54HC193	4-bit up/down counter	HCMOS	TIX					Aug-88				
ARSP	54HC266	Quad 2-input NOR gate	HCMOS	NSC					Mar-88	>60		UCB	
ARSP	54HC273	Octal D-type F/F	HCMOS	TIX					Dec-88	>120			
JPL/ARSP	54HC280	9-bit parity generator	HCMOS	TIX					Dec-88	>100			
ARSP	54HC299	8-bit shift/storage register	HCMOS	RCA					Mar-88	>120			
JPL/ARSP	54HC32	Quad 2-input OR gate	HCMOS	TIX					Mar-90	>100			
JPL	54HC373	Octal 3-state transparent latch	HCMOS	NSC	75					>75		UCB.	
ARSP	54HC373	Octal 3-state transparent latch	HCMOS	RCA					Mar-88	>120			
JPL/ARSP	54HC373	Octal 3-state transparent latch	HCMOS	RCA	>75					>120			
JPL	54HC373	Octal 3-state transparent latch	HCMOS	SPI	>75					>120			
JPL	54HC373	Octal 3-state transparent latch	HCMOS	STM					Aug-88	>80			
ARSP	54HC373	Octal 3-state transparent latch	HCMOS	STX	>75					>80			
JPL	54HC373	Octal 3-state transparent latch	HCMOS	TIX					Aug-88	>80			
ARSP	54HC374	Octal D-type F/F	HCMOS	MOT.	>75					>80		UCB	
ARSP	54HC374	Octal D-type F/F	HCMOS	TIX	60				Mar-90	>80			
JPL	54HC374	Octal D-type F/F	HCMOS	TIX					Dec-88	>80			
JPL	54HC390	Dual decade ripple counter	HCMOS	STM					Aug-88	>60			
ARSP	54HC390J	Dual decade ripple counter	HCMOS	TIX					Sep-89	>80			
JPL	54HC4046	Phase Lock Loop	HCMOS/bulk (3.5 µm).	NSC					Apr-95	>120		BNL	

Test Org.*	Device	Function	Technology	Mfr.	Effective SEU LET* Threshold	Device Xsection (cm^2)	Bits Tested	Bit Xsection (cm^2)	Test Date	LUth	LU Xsection (cm^2)	Fac.	Remarks 31-Aug-99
	Note: Entries in **RED** indicate data added since the 1997 Compendium.												
ARSP	54HC595J	8-bit register	HCMOS	TIX					Sep-89	120			
ARSP	54HCT 00	Quad NAND gate	HCMOS/TTL compat.	RCA									
ARSP	54HCT 04	HEX Inverter	HCMOS/TTL compat.	RCA									
ARSP	54HCT 08	Quad 2-input AND Gate	HCMOS/TTL compat.	RCA						>100			
ARSP	54HCT 10	Triple 3-input NAND gate	HCMOS/TTL compat.	RCA						>100			
ARSP	54HCT 27	Triple 3-input NOR gate	HCMOS/TTL compat.	RCA									
ARSP	54HCT 74	Dual D-type F/F	HCMOS/TTL compat.	RCA									
ARSP	54HCT109	Dual JK-type F/F	HCMOS/TTL compat.	RCA						>100			
ARSP	54HCT138	3 to 8 line decoder	HCMOS/TTL compat.	RCA						>75			
ARSP	54HCT154	4 to 16 line decoder/deMUX	HCMOS/TTL compat.	RCA					Mar-88	>80			
ARSP	54HCT163	4-bit binary counter	HCMOS/TTL compat.	RCA						>80			
ARSP	54HCT164	8-bit par. out shift register	HCMOS/TTL compat.	RCA						>80			
ARSP	54HCT165	8-bit shift register	HCMOS/TTL compat.	RCA						>80			
ARSP	54HCT174F	Hex D-type F/F	HCMOS/T	RCA	20	2.0E-04			May-89				
ARSP	54HCT373	Octal 3-state transparent latch	HCMOS/T	NSC	~75	1.0E-06			Dec-88	>120		UCB.	
ARSP	54HCT373	Octal 3-state transparent latch	HCMOS/T	TIX	~70	5.0E-06			Jan-91				
JPL	54HCT373C	Octal 3-state transparent latch	HCMOS/T	STX	>75				Jun-85				
JPL	54HCT373F	Octal 3-state transparent latch	HCMOS/T	RCA	>75				Dec-86				
ARSP	54HCT373F	Octal 3-state transparent latch	HCMOS/T	TIX	50	2.0E-05			May-89				
ARSP	54HCT393	Dual 4-bit counter	HCMOS/T	GEC	23	4.0E-05			Jun-92				
ARSP	54HCT393	Dual 4-bit counter	HCMOS/T	HAR	23	4.0E-05			Jun-92				
JH	54HCT4059	4 decade, Divide-by-N Counter	HCMOS/TTL compat.	RCA					1990				
ARSP	54HCT688	8-bit identity comparator	HCMOS/TTL compat.	RCA									
ARSP	54HCTS161	4-bit presettable counter	HCMOS/SOS	RCA	>75				Jun-88				
ARSP	54HCTS374	Octal D-type F/F	HCMOS/SOS	RCA	>75				Jun-88				
JPL	54L 73	4-bit JK-type F/F	Bipolar-LTTL	NSC	>37	2.0E-04		5.0E-05				UCB	
JPL	54L 73	4-bit JK-type F/F	Bipolar-LTTL	TIX	50							UCB	D/C 8250

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Test Org.*	Device	Function	Technology	Mfr.	Effective SEU LET* Threshold	Device Xsection (cm^2)	Bits Tested	Bit Xsection (cm^2)	Test Date	LUth	LU Xsection (cm^2)	Fac.	Remarks 31-Aug-99
	Note: Entries in **RED** indicate data added since the 1997 Compendium.												
JPL	54L 73	4-bit JK-type F/F	Bipolar-LTTL (old)	TIX	~30	1.0E-04		<2.5E-05				UCB	1974 vintage
JPL	54L 75	4-Bit Counter	Bipolar-LTTL	NSC	<37	1.0E-05		2.5E-06				UCB	
JPL/ARSP	54L 78	Dual JK-type F/F	Bipolar-LTTL	NSC	>37							Bevalac	No beam angle available.
JPL	54L 93	4-Bit Counter	Bipolar-LTTL (old)	TIX	12	4.5E-04		1.0E-04				BNL	1974 vintage
JPL	54L 93	4-Bit Counter	Bipolar-LTTL	TIX	30							BNL	D/C 8246
JPL	54L 95	4-bit par. in-out shift register	Bipolar-LTTL	NSC	<37	2.0E-04		5.0E-05				UCB	
JPL	54L 95	4-bit par. in-out shift register	Bipolar-LTTL	TIX	<37	2.0E-04		5.0E-05				UCB	
JPL	54LS 00	Quad NAND gate	Bipolar-LSTTL	SGN	<37							UCB	Transients with >200 mV; pulse width = 20-25 ns.
JPL	54LS 73	4-bit JK-type F/F	Bipolar-LSTTL	SGN	~4	8.0E-05		2.0E-05				UCB	
JPL	54LS 73	4-bit JK-type F/F	Bipolar-LSTTL	TIX	5				Dec-88			BNL	
JPL	54LS 73 (SA3318)	4-bit JK-type F/F	CMOS	SNL	>75								
JPL	54LS 74A	Dual D-type F/F	Bipolar-LSTTL	AMD	13							UCB	
MMS	54LS 74A	Dual D-type F/F	Bipolar-LSTTL	TIX	7	1.0E-04		2.5E-05	1992	>32		GANIL	Dufour, et al, 92IEEE Wrkshp Rec., pg 21.
JPL	54LS 95	Shift Reg.	Bipolar-LSTTL	SGN	11	6.0E-04		5.0E-05				UCB	
JPL	54LS109	Dual JK-type F/F	Bipolar-LSTTL	FAS	10	9.0E-05		2.3E-05				UCB	
ARSP	54LS109	Dual JK-type F/F	Bipolar-LSTTL	NSC	7	2.5E-05		1.6E-05		>32		UCB	
ARSP	54LS112	Dual JK-type F/F	Bipolar-LSTTL	MOT	6	1.0E-04		5.0E-05	Jun-92			UCB	
JPL	54LS163	4-bit binary counter	Bipolar-LSTTL	NSC	13	2.0E-04		5.0E-05				UCB	
JPL	54LS169	4-Bit Counter	Bipolar-LSTTL	AMD	<37							UCB	
ARSP	54LS169	4-Bit Counter	Bipolar-LSTTL	SGN	15	5.0E-05		1.3E-05				UCB	
ARSP	54LS173	4-bit D-type, 3-state register	Bipolar-LSTTL	SGN	12	2.0E-04		5.0E-05				UCB	
JPL	54LS194A	4-bit bidirectional shift register	Bipolar-LSTTL	TIX	5	8.0E-05		2.0E-05		25		UCB	
JPL	54LS373	Octal 3-state transparent latch	CMOS	SNL	>75					>100		UCB	
ARSP	54LS373	Octal 3-state transparent latch	Bipolar-LSTTL	TIX	15	2.0E-04		2.5E-05		>100		UCB	
JPL	54LS374	Octal D-type F/F	CMOS	SNL	~75					>100		UCB	
ARSP	54LS378	Hex D-type F/F	Bipolar-LSTTL	TIX	13	2.0E-04		3.3E-05				UCB	
JPL	54LS395	Shift Register	Bipolar-LSTTL	SGN	8							UCB	

Test Org.*	Device	Function	Technology	Mfr.	Effective SEU LET* Threshold	Device Xsection (cm^2)	Bits Tested	Bit Xsection (cm^2)	Test Date	LUth	LU Xsection (cm^2)	Fac.	Remarks 31-Aug-99
	Note: Entries in **RED** indicate data added since the 1997 Compendium.												
JPL	54LS398	Shift Register	Bipolar-LSTTL	SGN	<37	3.0E-04		5.0E-05				UCB	
ARSP	54S 74	Dual D-type F/F	Bipolar-Schottky	SGN	23	2.0E-05		1.0E-05				UCB	
ARSP	54S 74	Dual D-type F/F	Bipolar-Schottky	TIX	20	1.0E-04		5.0E-05	Jan-89			UCB	
JPL	54S169	4-Bit Counter	Bipolar-Schottky	AMD	>28								
JPL	54S169	4-Bit Counter	Bipolar-Schottky	AMD	>28							UCB	
JPL	54S374	Octal D-type F/F	Bipolar-Schottky	TIX	15							UCB	
JPL	54SC373	Octal 3-state transparent latch	CMOS	MTL	35	1.0E-06				>80			Near soft error threshold.
JPL	74 95	Shift Register	Bipolar-TTL	TIX	~75				May-81			UCB	SEU response expected to be the same as that of 5495.
GSFC	74FTC163374PV	3.3V/5V 16-Bit Register	CEMOS (low power)	IDT	~20				May-94	25	5.0E-04	BNL	Compare to IDT CEMOS transceiver
ARSP	74HC 00D	Quad NAND gate	HCMOS	RCA					Feb-90				
ARSP	74HC 04D	HEX Inverter	HCMOS	RCA					Feb-90				
ARSP	74HC 75D	4-bit bistable latch	HCMOS	RCA					Feb-90	>80			
ARSP	74LS 74	Dual D-type F/F	Bipolar-LSTTL	TIX	5	1.0E-04		5.0E-05		>80			
JPL	74LS 95	4-bit par. in-out shift register	Bipolar-LSTTL	TIX	<37	1.0E-04		2.5E-05		>120			
JPL	74LS162	Decade count up counter	Bipolar-LSTTL	TIX	<37	2.0E-04		5.0E-05		>120			
JPL	74LVQ244	3V Buffer	CMOS/epi	NSC					Apr-96	>120		BNL	Tested at 90 °C.
JPL	76L 70	Shift Register	Bipolar-LTTL	NSC	<37	3.0E-04		4.0E-05	May-81	>60			
JPL	93S 10	BCD decade counter	Bipolar-Schottky	FAS	<37	5.0E-06		1.3E-06		>85			
JPL	9407 (SA3268)	Data Register	CMOS (80 Kohm)	SNL	>55					>74			Development Part.
JPL	ADSP1016A	Multiplier	CMOS	ADI						<<37	4.0E-04	UCB	
JPL	CD4013B	D-type F/F	CMOS	RCA	>75				Jan-84	14		UCB	
JPL	**CD4014**	**Shift Register**	**CMOS**	**HAR**	**>120**				**Apr-96**	**>120**		**BNL**	**Tested @ 125deg. C. D/C 9403. Test of newer vintage CD4xxx.**
JPL	CD40160	Presettable decade counter	CMOS	FAS	>75				Jun-81	>60		UCB	
JPL	CD40161	Presettable binary counter	CMOS	RCA	>75				Jan-84	>60		UCB	
JPL	CD4018A	Presettable divide-by-N counter	CMOS	RCA					Jan-81	>80		UCB	No LU @ 10V using 120 MeV Kr (Range = 20µm).
ARSP	CD4021B	8-bit par. in/ser. out shift reg.	CMOS	RCA	>125					>100		UCB	
JPL	CD4027B	Dual JK-type F/F	CMOS	RCA	>75				Jan-84	>100		UCB	

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Test Org.*	Device	Function	Technology	Mfr.	Effective SEU LET* Threshold	Device Xsection (cm^2)	Bits Tested	Bit Xsection (cm^2)	Test Date	LUth	LU Xsection (cm^2)	Fac.	Remarks 31-Aug-99
	Note: Entries in **RED** indicate data added since the 1997 Compendium.												
JPL	CD4031	64-bit static shift register	CMOS	RCA	>75							UCB	
JPL	CD4049A	Inverting hex buffer/counter	CMOS	RCA					Jan-81	>116			
JPL	CD4049A	Inverting hex buffer/counter	CMOS	RCA					Jan-81	>80		UCB	No LU @ 10V using 120 MeV Kr (Range = 20µm).
JPL	CD4066B	Bilateral Switch	CMOS	RCA					Dec-87	>120		UCB	Tested at T=80 deg. C.
JPL	CD4081B	Quad 2-input AND	CMOS	RCA					Jan-81	>80		UCB	No LU @ 10V using 120 MeV Kr (Range = 20µm).
JPL	CD54HC4046	Phase Lock Loop	HCMOS/bulk-3.0 µm.	HAR					Apr-95	10 to 20		BNL	
ARSP	CO422	Clock Counter	CMOS	VTN					Apr-88	<36		UCB	
ARSP	CO422	Clock Counter	CMOS	VTN					Apr-88	>60		UCB	
JPL	F100331	D-FF (Master-Slave)	Bipolar/ECL(100K)	NSC	10	1.7E-04	1000		Jun-93	>85		BNL	Nichols et al, Jun 93.
ARSP	F100331	D-FF (Master-Slave)	Bipolar/ECL (1 µm epi)	NSC	~3	5.0E-04	2700			>65		UCB	Koga et al., 95IEEE TNS, No. 6, pg 1823. D/C 9220. F100K300 technology family.
MM	F100336	4-Stage Counter/shift register	Bipolar/ECL	NSC	27(10kHz)	1.0E-06			Apr-93	>74		BNL?	Tested at 1MHz. D/C 9127A.
ARSP	F100341	Shift register (8 F/F)	Bipolar/ECL (1 µm epi)	NSC	~3	1.0E-03	1000			>95		UCB	Koga et al., 95IEEE TNS, pg 1823. D/C 9220. F100K300 technology family.
ARSP/HAR	HD6434	Latch	CMOS	HAR						14	7.0E-05	UCB	
ARSP	HI546	16-channel MUX	CMOS	HAR					Mar-88	25			
ARSP	HI548	8-channel MUX	CMOS	HAR					Mar-88				
ARSP	HI549	4-channel differential MUX	CMOS	HAR					Mar-88				
ARSP	HI6208	Analog MUX	CMOS	HAR					1992				
GSFC	HS508RH	Analog MUX	HCMOS	HAR	110				Jun-93				LaBel, et al, 94IEEE Wrkshp Rec., pg 64.
GD	IDT7210	Multiplier Accumulator	CMOS	IDT					Apr-90		5.0E-07	Cf-252	LU cross section = 1.3E-5 cm2 @ 85 deg. C.
MMS	MC10531	D-FF	Bipolar/ECL	MOT	<32	1.0E-05		2.5E-06	1992	>116		GANIL	Dufour, et al, 92IEEE Wrkshp Rec., pg 21.
JH	P54PCT245	Logic	CMOS	PFS					1989	<40		BNL	
LIN	P54PCT245	Logic	CMOS	PFS					Apr-91	<27		BNL	
JPL	SA3294	Peripheral D-Latch	CMOS/bulk Twin Well	SNL	>120				Oct-88				Similar to 54LS373.
JPL	SA3295	Peripheral 3X8 Decoder	CMOS/bulk Twin Well	SNL	>120				Oct-88				Similar to 54LS138.
ESA	TLC555	Precision Timer	LinCMOS	TIX					1993	10 to 20	1.0E-04		H. Van Looy, ESA Rept (1993)
CNES	TMC2210	16-bit Mult./Accum.	CMOS	TRW					Nov-88	<36	5.0E-05	GANIL	Matra Rept. Nov 88
MMS	TMC2210	16-bit Mult./Accum.	CMOS	TRW						>61		GANIL	Dufour, et al, 92IEEE Wrkshp Rec., pg 21..

Test Org.*	Device	Function	Technology	Mfr.	Effective SEU LET* Threshold	Device Xsection (cm^2)	Bits Tested	Bit Xsection (cm^2)	Test Date	LUth	LU Xsection (cm^2)	Fac.	Remarks 31-Aug-99
	Note: Entries in **RED** indicate data added since the 1997 Compendium.												
		SRAMs											
ROCK	2147	4K x 1	NMOS	INT	16	6.5E-02							
ROCK	4044	Quad NAND	NMOS	TIX	<18	5.5E-02							
ROCK	4104	Voltage translator	NMOS	MOS	0.5	4.0E-02							
JPL	8155	I/O timer	NMOS	AMD	<37	4.0E-02				no			
JPL	8155	I/O timer	NMOS	INT	<37	6.0E-02				>120			
ARSP	8414		CMOS	FUJ	12	1.7E-02							
ROCK	10432		PMOS	ROC	<37	1.0E-02							
ARSP	29705	16 x 4	Bipolar TTL	AMD	6	4.0E-03							
ROCK	30222		CMOS/SOS	ROC	>75					>100			
JH	71256	32K x 8		HTC	4	1.0E-01		4.0E-07	Aug-90			BNL	Compare IDT71256.
GSFC	71256	32K x 8	CMOS-crossed-R. Two versions	UTM	>80				Dec-92	>120		BNL	LaBel. 1.2 µm technology. Possible noise. No valid upsets
JPL	93419	64 x 8	Bipolar TTL	FAS	<5	7.0E-03		>7.0E-06	Dec-91			UCB	Goka, 91IEEE TNS, No. 6, pg 1693 for orbital comparisons
NASDA	**93419**	**64 x 8**	**Bipolar TTL**	**FAS**									**Shimano, et al, 91IEEE TNS, No. 6, pg 1693.**
JPL	93422	256 x 4	Bipolar TTL	AMD	<1	4.0E-02		4.0E-05	Jun-87			UCB	Campbell, 91IEEE TNS, No. 6, pg. 1647. Gives CRRES data. Similar results @ BNL.
ROCK	93471		Bipolar TTL	FAS	<14	2.7E-02		7.0E-06				UCB	110 MeV argon.
GSFC	**628128**	**128K x 8**	**CMOS (1 µm). NMOS Periph.**	**HTC**	**1.45**				**1995**	**>60**		**BNL**	**LaBel, et al, 96IEEE Wrkshp Rec. pg 19. Address errors.**
GSFC	**628128**	**128K x 8**	**CMOS (1 µm). NMOS Periph.**	**HTC**	**3.38**				**1995**	**>60**		**BNL**	**LaBel, et al, 96IEEE Wrkshp Rec. pg 19. Bit errors.**
GSFC	**628128**	**128K x 8**	**CMOS (1 µm). NMOS Periph.**	**HTC**					**1995**				**LaBel, et al, 96IEEE Wrkshp Rec. pg 19. Address errors.**
ARSP	µPB10474	SRAM	Bipolar-ECL	NEC	<<3	1.0E-01	2000			>40			
ARSP	µPD43256A	32K x 8	CMOS/NMOS	NEC	3	4.0E-01			Mar-90			UCB	No latchup
NTT	µPD446	2K x 8	CMOS	NEC	<<18	1.6E-02		1.0E-06				TU	Latchup. Tested at Tokyo Univ.
NASDA	**µPD4464D-20**	**2K x 8**	**CMOS**	**NEC**					**1997**	**4.56**	**2.4E-01**	**var.**	**Goka, et al, 98IEEE TNS, No. 6, pg. 2771.**
IBM	2568CRH	32K x 8	RHCMOS (Manassas)	IBM	>100				Mar-93	>100		BNL	From IBM Rept on Space Station (DMS) - 3/93
ARSP	27LS00	256 x 1	Bipola -LSTTL	AMD	4	1.0E-02		4.0E-05				UCB	
JPL/ARSP	31L01		Bipolar LTTL	AMD	6	1.0E-03		1.5E-05				UCB	
SEI	**32C408BRP**	**512K x 8**	**CMOS**	**SEI**	**3.3**	**3.5E-05**			**1997**	**>117**		**BNL**	**Layton, et al, 98IEEE Wrkshp Rec., pg 170.**

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Test Org.*	Device	Function	Technology	Mfr.	Effective SEU LET* Threshold	Device Xsection (cm^2)	Bits Tested	Bit Xsection (cm^2)	Test Date	LUth	LU Xsection (cm^2)	Fac.	Remarks 31-Aug-99
	Note: Entries in **RED** indicate data added since the 1997 Compendium.												
NASDA	**38510/91901XCR**	**64K**	**CMOS/epi**	**NEC**	**16.6**	**6.4E-02**		**1.0E-06**	**1997**	**>70**		**TIARA**	**Goka, et al, 98IEEE TNS, No. 6, pg. 2771.**
NASDA	**38510/92001XB**	**256K**	**CMOS**	**HTC**	**7.2**	**5.1E-02**		**2.0E-07**	**1997**	**>62**		**Var.**	**Goka, et al, 98IEEE TNS, No. 6, pg. 2771.**
JPL	4736B		LOC/MOS/epi	PHL	~100							UCB	
ARSP	51C67		CMOS/epi	INT	2	1.0E-02		6.0E-07				UCB	
JPL	51C98	64K x 8	CMOS/epi	INT	3	6.0E-02		1.0E-06	Oct-90	40		UCB	
ARSP	54F189	16 x 4	Bipolar TTL/F	NSC	3	2.0E-03			May-90			UCB	No LU
ARSP	54S189	16 x 4	Bipolar STTL	AMD	3	5.0E-05			Feb-90			UCB	No LU
ARSP	54S189	16 x 4	Bipolar STTL	SGN	5	1.5E-03		2.4E-05				UCB	
ARSP	54S201		Bipolar STTL	SGN	5	9.0E-03		3.5E-05				UCB	
GSFC	**5C1008FE-M**	**128K x 8**	**CMOS**	**AUS**	**<3.38**	**2.0E-01**			**1997**	**>50**		**BNL**	**O'Bryan, et al, 98IEEE Wrkshp Rec., pg 39. Multi-bit errors also seen.**
CNES	61CD16	2K x 8	CMOS/epi (EPIC)	TIX					1990	<13	6.0E-03	IPN	Chapuis
CNES	61CD16	2K x 8	CMOS/epi EPIC	TIX		4.0E-02		2.5E-06	Aug-90	<13	8.0E-03	IPN	Chapuis
CNES	61CD64S	8K x 8	CMOS/epi (EPIC)	TIX						>116		GANIL	
MHS	65162E	2K x 8	CMOS	MHS	3		120			>100			TEMIC/Matra MHS Radiation Evaluation Results Table, July 1996.
MHS	65262E	16K x 1	CMOS	MHS	3		120			>100			TEMIC/Matra MHS Radiation Evaluation Results Table, July 1996.
MHS	65656F	32K x 8	CMOS	MHS	4		30			>100			TEMIC/Matra MHS Radiation Evaluation Results Table, July 1996.
MHS	65664E	8K x 8	CMOS	MHS	6		20			>100			TEMIC/Matra MHS Radiation Evaluation Results Table, July 1996.
MHS	65687E	64K x 1	CMOS	MHS	6		20			>100			TEMIC/Matra MHS Radiation Evaluation Results Table, July 1996.
MHS	65697F	256K x 1	CMOS	MHS	4		30			>100			TEMIC/Matra MHS Radiation Evaluation Results Table, July 1996.
MHS	67005E	8K x 8 Dual Port	CMOS	MHS	4		100			>100			TEMIC/Matra MHS Radiation Evaluation Results Table, July 1996.
MHS	67024E	4K x 16 Dual Port	CMOS	MHS	4		100			>100			TEMIC/Matra MHS Radiation Evaluation Results Table, July 1996.
MHS	67025E	4K x 16 Dual Port	CMOS	MHS	7		150			>100			TEMIC/Matra MHS Radiation Evaluation Results Table, July 1996.
MHS	67130E	1K x 8 Master Dual Port	CMOS	MHS	4		100			>100			TEMIC/Matra MHS Radiation Evaluation Results Table, July 1996.
MHS	67132E	2K x 8 Master Dual Port	CMOS	MHS	4		100			>100			TEMIC/Matra MHS Radiation Evaluation Results Table, July 1996.
MHS	67140E	1K x 8 Master Dual Port	CMOS	MHS	4		100			>100			TEMIC/Matra MHS Radiation Evaluation Results Table, July 1996.
MHS	67142E	2K x 8 Slave Dual Port	CMOS	MHS	4		100			>100			TEMIC/Matra MHS Radiation Evaluation Results Table, July 1996.
GSFC	70V25	8K x 16 Dual Port	CMOS	IDT	<3.46			5.0E-07	Jul-94	>80		BNL	LaBel, et al, 96IEEE Wrkshp Rec., pg 19. Some multiple-bit errors.

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Test Org.*	Device	Function	Technology	Mfr.	Effective SEU LET* Threshold	Device Xsection (cm^2)	Bits Tested	Bit Xsection (cm^2)	Test Date	LUth	LU Xsection (cm^2)	Fac.	Remarks 31-Aug-99
	Note: Entries in **RED** indicate data added since the 1997 Compendium.												
JPL	82S19	64 x 9	Bipolar-STTL	SGN	<5	>1.0E-02		>1.0E-05				CIT	29 MeV Oxygen
JPL	82S212	256 x 9	Bipolar-STTL	SGN	1	2.0E-02		1.0E-05	Jun-87			BNL	Campbell, 91IEEE TNS, No. 6, pg. 1647. Gives CRRES data.
ARSP	93L422	256 x 4	Bipolar-LTTL	AMD	<1	1.5E-02		1.5E-05	Dec-91			UCB	Campbell, 91IEEE TNS, No. 6, pg. 1647. Gives CRRES data.
JPL	93L422	256 x 4	Bipolar-LTTL	AMD	<1	4.0E-02		4.0E-05	Dec-91			UCB	Compare to previous entry. Remarks for TTL 93422 apply
JPL/ ARSP	93L422	256 x 4	Bipolar-LTTL	FAS	1.8	2.0E-02		2.0E-05	Jul-86			UCB	See 89IEEE TNS, pg 2283 & 91IEEE TNS, No. 6, pg 1708.
JPL/ ARSP	93L425	1K x 1	Bipolar-LTTL	FAS	<37	1.5E-02		1.5E-05				UCB	
ARSP	99C641	256 x 4	CMOS	AMD	~1	3.0E-01		5.0E-06	Mar-87			UCB	
JPL	AM21L47	4K x 1	NMOS	AMD	1.6	4.1E-01		1.0E-04	Aug-85			UCB	Campbell, 91IEEE TNS, No. 6, pg. 1647. Gives CRRES data.
ARSP	AM9122	256 x 4	Bipolar-LTTL	AMD	2	4.0E-02		4.0E-05				UCB	A variant of the 93L422.
JPL	AM92L44	4K x 1	NMOS	AMD	1.6	4.1E-01		1.0E-04	Aug-85			UCB	Campbell, 91IEEE TNS, No. 6, pg. 1647. Gives CRRES data.
MMS	**AS5C4008CW-35E**	**512K x 8**	**CMOS/epi, 0.5 µm feature**	**ASI**	**~1**			**8.0E-07**				**CYC**	**Poivey, et al, 98IEEE Wrkshp Rec., pg 68. D/C 9731. MOT chips packaged by Austin.**
GSFC	**AS5C512K8**	**512K x 8**	**CMOS**	**AUS**	**<3.38**	**1.0E-03**			**1997**			**BNL**	**O'Bryan, et al, 98IEEE Wrkshp Rec., pg 39. Multi-bit errors also seen.**
JPL/ ARSP	CD4061		CMOS	RCA	~75							UCB	
JPL/ARSP/ ROCK	CDP1821	1K x 1	CMOS/SOS	RCA	145							UCB	
JPL/ ROCK	CDP1822	256 x 4	CMOS/SOS	RCA	<216							UCB	
ROCK	CDP1825	64 x 8	CMOS/SOS	RCA	<37	4.0E-04		1.0E-07				UCB	
ARSP	CMM5104	4K x 1	CMOS/SOS	RCA	50							UCB	
ARSP/ ROCK	CMM5114	1K x 4	CMOS/SOS	RCA	58				Dec-91			UCB	Wilkinson, et al, 91IEEE TNS, No. 6, pg 1708. TDRS data.
JPL/ ARSP	CMM6167	16K x 1	CMOS/SOS	RCA	15	4.0E-04		3.0E-08 - 1.0E-07	Feb-89			UCB	Bit X-section = 10 @ LET = 120. Hi temp data available. 10/87, 6/88, & 2/89.
NRL	Comp. Heterostruct.	1K x 1	C-HIGFET (1 µm GaAS)	HON	~1			7.7E-07		>120		BNL	C-HIGFET SEU rates are 2 to 3 orders < than GaAs MESFETs. Proton data exists.
CNES	CXK581000	128K x 8	CMOS/NMOS	SNY	<1.7			7.0E-09 - 7.0E-08				IPN	Underwood, et al, 93IEEE Wrkshp Rec., pg 85. Bit X-section pattern depend. Proton data exists.
MMS	**CXK581000BP-10LL**	**128K x 8**	**CMOS**	**SNY**	**~2**			**1.0E-08**	**1997**	**>68**		**CYC**	**Poivey, et al, 98IEEE Wrkshp Rec., pg 68.**
ARSP	CXK581000P-10L	128K x 8	CMOS/NMOS	SNY	3	8.0E-02			Feb-90	55	2.0E-05	UCB	Includes multiple upsets.
JPL	CXK581000P-10LL	128K x 8	CMOS/NMOS	SNY	1.4	1.8E-01			Mar-93	15 to 38		BNL	Multiple errors suggested.
CNES	CXK581001	128K x 8	DC:9150/9151	SNY	<1.7			2.0E-09 - 4.0E-08				IPN	Underwood, et al, 93IEEE Wrkshp Rec., pg 85. Bit X-section pattern depend. Proton data exists.
ARSP	CXK581001	128K x 8	CMOS/NMOS	SNY	3	1.5E-01			Oct-92	30	5.0E-05	UCB	
ARSP	CXK58255	32K x 8	CMOS	SNY	6	1.0E-01			May-90	25	1.0E-03	UCB	Include multiple errors.

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Test Org.*	Device	Function	Technology	Mfr.	Effective SEU LET* Threshold	Device Xsection (cm^2)	Bits Tested	Bit Xsection (cm^2)	Test Date	LUth	LU Xsection (cm^2)	Fac.	Remarks 31-Aug-99
	Note: Entries in **RED** indicate data added since the 1997 Compendium.												
CNES	CXK58257	32K x 8	CMOS	SNY	<3							IPN	Duzellier, et al, 93IEEE Wrkshp Rec., pg. 36. Also has proton data.
JPL	CXK58258AP-1020	SRAM	CMOS	SNY	3	1.0E-03			Apr-96	40	2.0E-06	BNL	
ARSP	CY100E474	SRAM	Bipolar/ECL	CYP	~3	1.0E-02		3.7E-06		>60		UCB	Koga, et. al., 95IEEE TNS, No. 6, pg 1823
ARSP	CY7C150	1K x 8	CMOS	CYP					Jun-88	<30	1.0E-05	UCB	
GD	CY7C185	8K x 8	CMOS	CYP					Apr-90		8.0E-05	Cf-252	Cross section =- 2.0E-04 @ 85 °C.
ARSP	CY7C189	16 x 4	CMOS	CYP	1	2.0E-04			May-90	8	2.0E-04	UCB	
JPL	CY7C199	32K x 8	CMOS	CYP	1.5	3.0E-01			Mar-94	10	5.0E-04	BNL	Upset cross section @ LET = 15.
ARSP	CYPC128A	2K x 8	CMOS/NMOS	CYP	2	7.0E-03		4.0E-07	Dec-92	10	1.0E-04	UCB	
CNES	D431000	128K x 8	CMOS	NEC	<3				1993			IPN	Underwood, et al, 93IEEE Wrkshp Rec., pg 85. Double hits. Proton data exists. D/C 9137
CNES	D43256	32K x 8	CMOS	NEC	<3				1993			IPN	Underwood, et al, 93IEEE Wrkshp Rec., pg 85. Double hits. Proton data exists. D/C 9035
ESA	D4464	64K x 4	CMOS	NEC	11				Dec-91			HARW	Goka, 91IEEE TNS, No. 6, pg 1693. Proton LU, McNulty, 93IEEE TNS, No. 6, pg. 1647.
ESA	D4464D	64K x4	CMOS	NEC					1992	2	1.5E-02	HARW	LU cross section @ saturation (LET = 12)
LIN	DPS92256	32K x 8	Densepac	HTC	<1.4				Aug-90	>54		BNL	
LIN	DPS92256	32K x 8	Densepac	SNY	~3				Aug-90	<26		BNL	
LIN	DPS92256G	32K x 8	CMOS	HTC					1991	<27		BNL	Sferrino
ARSP	EDH8832C	32K x 8	NMOS/CMOS	EDI	3	5.0E-01		2.0E-06	Dec-87	30	2.0E-03	UCB	
ESA	EDH8832C	32K x 8	NMOS/CMOS	EDI/MIT	~2			1.0E-06	Dec-91			IPN	Adams, 91IEEE TNS, No. 6, pg 1686.
CLEM	HC5517A	2K x 8	CMOS	TIX	5	5.0E-06			Dec-91			BNL	McNulty, 91IEEE TNS, No. 6, pg. 1463. Cross section @ LET = 24.
HON	HC6116	2K x 8	CMOS with variable R.	HON	14			1.0E-06	Jun-92			BNL	Stassinopoulos, 91IEEE, NS-39, No. 3, p 450.
JPL	HC6116CHEC	2K x 8	CMOS (CMOS compat)	HON	28	6.0E-02		4.0E-06	Jun-88			UCB	Feb & June 1988. High temperature data exists.
JPL	HC6116CHET	2K x 8	CMOS (TTL compat)	HON	14	6.0E-02		4.0E-06	Jun-88			UCB	Same response as above.
ARSP	HC6116KSH-T	2K x 8	CMOS	HON	25	2.0E-02			Dec-89			UCB	No LU
JPL/ARSP	HC6167R	16K x 1	CMOS with R = 435 Kohms	HON	>120				Jul-88			BNL	No LU @ high temp. Similar results @ UCB.
HON	HC6216	2K x 8	CMOS with variable R.	HON	25 to 40			8.0E-07				BNL	Same as Hon test of HC6116. HC6216 is a variant of HC6116
HON	HC6364	8K x 8	CMOS/epi (4 µm); 500 kohm	HON	>90				Sep-89			BNL	Data at higher temps & with other resistors.
HON	HC6364	8K x 8	CMOS/epi	HON	<18				1993				McNulty, 93IEEE TNS, No. 6, pg 1947.
JPL	HC6364	8K x 8	CMOS/epi	HON	36	2.0E-02			Mar-93	>84		BNL	SEU data at higher T. Comparable HON data is SEU LET_{th} = 56.

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Test Org.*	Device	Function	Technology	Mfr.	Effective SEU LET* Threshold	Device Xsection (cm^2)	Bits Tested	Bit Xsection (cm^2)	Test Date	LUth	LU Xsection (cm^2)	Fac.	Remarks 31-Aug-99
	Note: Entries in **RED** indicate data added since the 1997 Compendium.												
HON	HC6856	32K x 8	RICMOS IV [R = 108K]	HON	40			1.0E-07	Nov-91			BNL	Test for variations of Resistance and temperature @ 2.7 µm. epi. HON Rept. 11/91
HON	HC6856	32K x 8	RICMOS IV [R = 335K]	HON	>160				Nov-91				Test for variations of Resistance and temperature @ 2.7 µm. epi. HON Rept. 11/91
US	HM1-65162-2	2K x 8	CMOS/epi	HAR	<3.6	1.0E-01			1991			GSI	Dreute, RADECS 91, pg 505. X-section @ 62. Very high E. Multiple bit errors.
JPL	HM1-6562B	1K x 1	CMOS	HAR	~100							UCB	
ARSP	HM6116	2K x 8	NMOS	HTC	4	1.0E-02		6.3E-07	Jun-87	>10	4.0E-03	UCB	
ESA	HM6116	2K x 8	CMOS	HTC	5			3.0E-06	Dec-90	<13	3.0E-04	IPN	D/C 88. Proton data exists.
ESA	HM62256	32K x 8	CMOS	HTC	3			2.0E-06	1993			IPN	Harboe-Sorensen, et al, 93IEEE TNS. No. 6, pg 1498. D/C 8641 & 8845. Proton data exists
CNES	HM62256R	32K x 8	CMOS	HTC	<1.7	3.0E-06		3.0E-06	1993			IPN	Underwood, et al, 93IEEE Wrkshp Rec., pg. 36. D/C 9303. No LU. Also has proton data.
CNES	HM62382H	32K x 8	CMOS	HTC	<1.7	4.0E-07		4.0E-07	1993			IPN	Underwood, et al, 93IEEE Wrkshp Rec., pg. 36. D/C 9303. No LU. Also has proton data.
ESA	HM6264	8K x 8	CMOS	HTC	~5			1.5E-06	Dec-93	<13	1.0E-03	BNL	Harboe-Sorensen, et al, 93IEEE TNS, No. 6, pg 1498. D/C 8431. Proton data exists
ESA	HM6264A	8K x 8	CMOS	HTC	~5			1.5E-06	Dec-93		1.0E-03	IPN	Harboe-Sorensen, et al, 93IEEE TNS, No. 6, pg 1498. D/C 8901. Proton data exists
MMS	HM628128	128K x 8	CMOS/epi	HTC					1993	>110		GANIL	Beaucour, 93IEEE Wrkshp Rec., pg 20. Hard Errors.
GSFC	HM628128	128K x 8	CMOS/epi	HTC	<1.4	3.3E+00			May-93	>110		BNL	LaBel, et al, 94IEEE Wrkshp Rec., pg 64. Dynamic test. Multiple bit hits.
GSFC	HM628128	128K x 8	CMOS/epi	HTC	<1.4	2.0E-01			May-93	>110		BNL	LaBel, et al, 94IEEE Wrkshp Rec., pg 64. Static test. Multiple bit hits.
ESA	HM628128	128K x 8	CMOS	HTC	~3			4.0E-07	1993			IPN	Harboe-Sorensen, et al, 93IEEE TNS, No. 6, pg 1498. D/C 9009. Proton data exists.
JPL	HM628128	128K x 8	NMOS/CMOS	HTC	4	6.0E-01		6.0E-07	Mar-90	80		UCB	
ARSP	HM628128	128K x 8	NMOS/CMOS	HTC	4	6.0E-01		6.0E-07	Jun-05	>127		UCB	Koga, et al, 93IEEE Wrkshp Rec., pg 1941.
GSFC	HM628128	128K x 8	CMOS & NMOS periph. (1 µm)	HTC	~1.4							BNL	
MMS	**HM628128BLP-7**	**128K x 8**	**Hi CMOS 0.8 µm feaures. Rev B**	**HTC**	**~2**			**3.0E-07**	**1997**			**CYC**	**Poivey, et al, 98IEEE Wrkshp Rec., pg 68. D/C 9713**
ESA	HM628512	512K x 8	CMOS	HTC	~2			6.0E-07				BNL	Harboe-Sorensen, et al, 93IEEE TNS, No. 6, pg 1498. D/C 9009. Proton data exists.
GSFC	HM628512	512K x 8	Hi-CMOS/epi. 0.5 µm features.	HTC	~1.5	1.3E+00		3.0E-07	Sep-92	>90		BNL	LaBel, et al, 94IEEE Wrkshp Rec., pg 64. Proton data exists.
MMS	**HM628512ALP-7**	**512K x 8**	**Hi CMOS 0.5 µm feaures. Rev A**	**HTC**	**~2**			**2.0E-07**	**1997**			**CYC**	**Poivey, et al, 98IEEE Wrkshp Rec., pg 68. D/C 9705**
JPL/ARSP/ HAR/ESA	HM6504	4K x 1	CMOS	HAR	5	5.0E-03		1.3E-06	Oct-87	13	1.0E-04	UCB	Also tested at IPN 12/90.
JPL/ARSP	HM6508	1K x 1	CMOS	HAR	15	1.0E-02		1.0E-05				UCB	Latchup.
ROCK	HM6508	1K x 1	CMOS	HAR	38	2.0E-03		2.0E-06				UCB	Latchup.
JPL/ARSP	HM6508RH	1K x 1	CMOS/epi	HAR	>37	4.0E-03		4.0E-06				UCB	Cross section @ high LET.
ARSP	HM6508RH	1K x 1	CMOS/epi & R = 20Kohm	HAR	>120							UCB	

Test Org.*	Device	Function	Technology	Mfr.	Effective SEU LET* Threshold	Device Xsection (cm^2)	Bits Tested	Bit Xsection (cm^2)	Test Date	LUth	LU Xsection (cm^2)	Fac.	Remarks 31-Aug-99
	Note: Entries in **RED** indicate data added since the 1997 Compendium.												
ARSP	HM6514	1K x 4	CMOS	HAR	10	2.0E-02		5.0E-06				UCB	Latchup
JPL/ARSP/ ESA	HM6516	2K x 8	CMOS	HAR	4	3.0E-02		2.0E-06	Mar-88	17	6.0E-04	UCB	Also tested @ IPN 12/90
JPL	HM6516	2K x 8	CMOS/epi (7 µm)	HAR	10	5.0E-02		3.0E-06	Feb-87	>37		UCB	Nichols, 87IEEE TNS, No. 6, pg 1800. Also tested at BNL
JPL/HAR	HM6516	2K x 8	CMOS/epi (12 µm)	HAR	<<6	2.0E-02		1.2E-06	Apr-87	~37		UCB	See IEEE ref. above. Also Hughes tested with Cf-252 - no LU.
SOR	HM65162	2K x 8	CMOS/no epi	HAR	3.5 to 4	5.0E-02			1995	4.5 to 8.5	2.0E-02	KA	Barak, et al, RADECS95, pg 321. Low energy ions. D/Cs 85, 86, 91.
JPL	HM65162	2K x 8	CMOS/epi	HAR					Apr-87	<<37	>>0.003	UCB	
CNES	HM65162	2K x 8	CMOS/epi	MHS					Feb-90	>37			Same tech. as HM65262.
CNES	HM65262	16K x 1	CMOS	MHS					Oct-89	<<37	4.0E-03	GANIL	
CNES	HM65262	16K x 1	CMOS/bulk	MHS					Feb-90	<16	6.0E-03	GANIL	
CNES	HM65262	16K x 1	CMOS/epi	MHS	3	9.0E-02			Feb-90			GANIL	Also tested at IPN.
JPL/ARSP	HM6551	256 x 4	CMOS	HAR	60					140			Kr at 75°C.
JPL	HM6551RH	256 x 4	CMOS/epi	HAR	~75								
CERT	HM65641	8K x 8	CMOS/epi	MHS	4	2.0E-01			1991	>72		IPN	Falguere, RADECS 91, p 479.
CNES	HM65641	8K x 8	CMOS/epi	MHS					Nov-90	<55		IPN	Chapuis, ESA Conf 11/90
CNES	HM65641	8K x 8	CMOS/epi (12 µm)	MHS	2.5	2.0E-01		3.0E-06	Dec-90	~50	4.0E-04	IPN	Chapuis, et al, 90IEEE TNS, No. 6, pg. 1839. D/Cs 8930 & 8933. Also tested @ GANIL.
MMS	HM65656	32K x 8	SCMOS/epi	MHS					1992	>140		GANIL	Dufour, et al, 92IEEE Wrkshp Rec., pg 21.
CNES	HM65656	32K x 8	SCMOS/epi	MHS	1.7	1.0E-01		3.0E-06	1993			IPN	Duzellier, et al, 95IEEE TNS, No. 6, pg 1797. High vs medium energy beam study. Comparison studies done at Saturne (France).
CERT/ CNES	HM65656	32K x 8	SCMOS/epi [high-performance]	MHS	5	1.0E-01	300						
SNL	**HM65656**	**32K x 8**	**CMOS, 0.8µm, rad-tolerant**	**MHS**	**~1**	**~1.5E-01**			**1997**			**BNL**	**Dodd, et al, 98IEEE TNS, No. 6, pg. 2483.**
MMS	HM65664	8K x 8	SCMOS/epi RT	MHS					1992	>140		GANIL	Dufour, et al, 92IEEE Wrkshp Rec., pg 21.
CNES	HM65664	8K x 8	SCMOS/epi [high-performance)	MHS	6	4.0E-01			Aug-91	>50		IPN	Final process. Aug. 91.
JSC	HM65664	8K x 8	SCMOS/epi [high-performance)	MHS	5			3.0E-07	Dec-90	>116		BNL	Also tested @ GANIL and IPN
CERT	HM65664	8K x 8	SCMOS/epi [high-performance)	MHS	5	4.0E-01			1991	>55		IPN	Falguere, RADECS 91, p 479.
JPL/ARSP	HS6504RH	4K x 1	CMOS/epi (rad hard)	HAR	36	1.2E-03		3.0E-07	Jun-88			UCB	Special JPL test of four epi thicknesses
ARSP	HS6504RH	4K x 1	CMOS/epi RH (R = 20 Kohm)	HAR	>80							UCB	
JPL	HS6504RRH	4K x 1	CMOS/epi RH (R = 200 kohm)	HAR	87				May-87			UCB	
ARSP	HS6504RRH	4K x 1	CMOS/epi RH (R = 200 kohm)	HAR	40	6.0E-08						UCB	Address latch only errors.

Test Org.*	Device	Function	Technology	Mfr.	Effective SEU LET* Threshold	Device Xsection (cm^2)	Bits Tested	Bit Xsection (cm^2)	Test Date	LUth	LU Xsection (cm^2)	Fac.	Remarks 31-Aug-99
	Note: Entries in **RED** indicate data added since the 1997 Compendium.												
ARSP	HS6514RRH	1K x 4	CMOS & R = 200 Kohm	HAR	>80							UCB	
JPL/ARSP	HS65262RH	16K x1	CMOS/epi	HAR	20	1.0E-02		6.0E-07				UCB	
ARSP	HS65262RRH	16K x 1	CMOS/epi & R=?	HAR	>75							UCB	
ARSP	HS65C162	2K x 8	CMOS	HAR	10	4.0E-02				60		UCB	
JPL	HS65C262RRH	16K x1	CMOS/epi (CMOS compat.)	HAR	~40				Jul-88			UCB	Transients
JPL	HS65T262RRH	16K x1	CMOS/epi (TTL compat.)	HAR	20	4.0E-06			Dec-87			UCB	Transients
JPL	HX6364	8K x 8	CMOS/SOI	HON	>90				May-91	>90		BNL	Tested at 125 deg. C
JPL	IBM 6401	64K x 1	CMOS/epi	IBM	>115				Jun-92	>115		BNL	Development SRAM.
ARSP/IBM	IBM Development RH		RHCMOS-E (CMOS/epi)	IBM	>110				1992	>110		BNL	Brown,et al, 92IEEE Wrkshp Rec., pg 72. Up to 125 deg. C. Also tested at UCB.
IBM	IBM Development RH		RHCMOS-E (CMOS/epi)	IBM	12			1.0E-06		>120		BNL	WP-2 (Jim Pollock).
JPL/ARSP	IDT6116	2K x 8	NMOS/CMOS	IDT	6	6.0E-02		4.0E-06	Oct-87			BNL	Latchup.
JPL/ARSP	IDT6116RH	2K x 8	NMOS/CMOS with epi	IDT	3	6.0E-02		4.0E-06		100		UCB	Also tested at BNL
JPL/ARSP	IDT6116V	2K x 8	CMOS	IDT	6	2.5E-02		1.6E-06	Feb-87	>120		BNL	Series 2A development RH part. Also tested @ UCB 6/87
ARSP	IDT6167	16K x 1	NMOS/CMOS	IDT	3	4.0E-02		2.5E-06				UCB	Latchup
ARSP	IDT6167X	16K x 1	NMOS/CMOS	IDT	5	2.6E-02		1.7E-06	Jun-87	>120		UCB	Rad Hard Device.
GSFC	IDT70324L	2K x 8	CEMOS (low power)	IDT					Jun-94	>90		BNL	LaBel.
JPL/ARSP	IDT7052	2K x 8	NMOS/CMOSV	IDT	4	8.0E-02		5.0E-06	Oct-92	>100		UCB	
ARSP/JH	IDT71256	32K x 8	NMOS/CMOS	IDT	2.5	2.0E-01			Aug-90	15	7.0E-05	UCB	Also tested at Bevalac (1993) RADECS 93.
ARSP	IDT71256 (Rad Hard)	32K x 8	NMOS/CMOS	IDT	3	1.0E-01			Sep-88	>120		UCB	Up to 90 deg C.
CNES	IDT7134	4K x 8	CMOS	IDT	<1.7			3.0E-06	1993	12	7.0E-04	IPN	Duzellier, et al, 93IEEE Wrkshp Rec., pg 36. D/C ES. Proton data exists.
JH	IDT7134RT	4K x 8	CMOS	IDT					1991	<<37		BNL	Kinnison
ARSP	IDT7164	8K x 8	NMOS/CMOS	IDT	3	8.0E-02		1.3E-06	Jun-87	>120		UCB	Rad Hard Device.
ARSP	IDT7164	8K x 8	NMOS/CMOSV	IDT	3	1.0E-01		1.5E-06	Oct-92	8	8.0E-03	UCB	
ARSP	IDT71681	4K x 4	NMOS/CMOS	IDT	2	1.2E-01		7.5E-06		>11		UCB	
ARSP	IDT71681RH	4K x 4	NMOS/CMOS with epi	IDT	5	2.6E-02		2.0E-06				UCB	
BREL	IDT7187	64K x 1	NMOS/CMOS	IDT					Dec-90	6	5.0E-04		Tested at unknown van de Graaff. 90IEEE-TNS.
ARSP	IDT7187	64K x 1	NMOS/CMOS	IDT	5	4.0E-02		6.3E-07	Jun-87				Rad Hard Device. Compare above

Test Org.*	Device	Function	Technology	Mfr.	Effective SEU LET* Threshold	Device Xsection (cm^2)	Bits Tested	Bit Xsection (cm^2)	Test Date	LUth	LU Xsection (cm^2)	Fac.	Remarks 31-Aug-99
	Note: Entries in **RED** indicate data added since the 1997 Compendium.												
JPL	IM6518	1K x 1	CMOS	INL	<37	3.0E-03		3.0E-06				UCB	
ARSP	IM65X08		CMOS	INL	<37	3.0E-03		3.0E-06				UCB	
ARSP	IM65X18		CMOS	INL	<37	3.0E-03		3.0E-06					
ARSP	IMS1600SL55	64K x 1	NMOS	ISM	<3	>2.0E-01			Mar-90	15	2.0E-03	UCB	
IBM	IMS1601EPI	64K x 1	CMOS non rad-hard	ISM	~2	4.0E-01			Oct-94	>60		UCB	Shinn, et al, 95IEEE TNS, pg 2017. Includes multibit errors using data of T. Scott (IBM)
IBM	IMS16-1EPI	64K x 1	CMOS/epi	SGS	3	3.0E-01			Jun-88	>60		UCB	T. Scott. Proton data exists.
ARSP	IN1600	64K x 1	NMOS/CMOS	ISM	~3	8.0E-01			Jun-87	<30	7.0E-03	UCB	Includes multibit errors. Also tested at ESTEC.
ARSP	IN1601	64K x 1	NMOS/CMOS	ISM	2	5.0E-01		8.0E-06	Mar-87	5	4.0E-04	UCB	Also tested at ESTEC.
CERT	IN1630SL	32K x 8	NMOS/CMOS	ISM	1	4.0E-01			1991	>72		IPN	Falguere, RADECS 91, p479. Double bit errors per data byte.
MMS	**IS61C1024-20M**	**128K x 8**	**CMOS (0.5 µm)**	**ISS**	**~2**			**1.5E-06**	**1997**	**>68**		**CYC**	**Poivey, et al, 98IEEE Wrkshp Rec., pg 68.**
JPL	KM684002	512K x 8	CMOS	SAM					Jan-97	>87		TAM	
MMS	**KM684002AJ-17**	**512K x 8**	**CMOS/epi, 0.5µm feature, Rev A**	**SAM**	**~1**			**1.0E-07**	**1997**			**CYC**	**Poivey, et al, 98IEEE Wrkshp Rec., pg 68.**
ARSP	L6116	2K x 8	CMOS/NMOS	LDI	5	8.0E-03		5.0E-07	Dec-92	15	1.0E-03	UCB	
JPL	L7C199DC-35	SRAM	CMOS	LDI					Apr-96				
SNL	**M65608**	**128K x 8**	**CMOS, 0.5µm, commercial**	**MHS**	**~1**	**1.0E-01**			**1997**			**BNL**	**Dodd, et al, 98IEEE TNS, No. 6, pg. 2483.**
SNL	**M65608E**	**128K x 8**	**CMOS, 0.5µm, rad-tolerant**	**MHS**	**~2**	**8.0E-02**			**1997**			**BNL**	**Dodd, et al, 98IEEE TNS, No. 6, pg. 2483.**
SNL	**M65964**	**64K test vehicle**	**CMOS, 1.0µm, rad-tolerant**	**MHS**	**~1**	**1.0E-01**			**1997**			**BNL**	**Dodd, et al, 98IEEE TNS, No. 6, pg. 2483.**
JPL	MA6116	2K x 8	CMOS/SOS	MED	>120				Apr-88			UCB	Hard technology.
ARSP	MA6116	2K x 8	CMOS/SOS	MED	43	1.0E-03			Apr-88	>90		UCB	
ESA	MA6116	2K x 8	CMOS/SOS	MED	32			8.0E-08				UCB	
ESA	MA6167	16K x 1	CMOS/SOS (3 µm)	MED	~40				1992			UCB	92IEEE TNS preprint.
CNES	MA9167	16K x 1	CMOS/SOS (1.5 µm)	MED	>72				Feb-90			IPN	
ESA	MA9187	64K x 1	CMOS/SOS	MED	60			>2.0E-08				UCB	
ESA	MARS94 Flight Part	32K x 8	CMOS Process SO6A	MCN	~1.5			5.0E-08	1993	>85		BNL	Harboe-Sorensen, RADECS 93 pg. 490.
CNES	MB81C81	256K x 1	CMOS tristate	FUJ					Feb-90	>114		IPN	
NTT	MB8401	1K x 1	CMOS	FUJ	18	2.0E-03		2.0E-06				TU	Tested at Toyko University.
JPL	MB8404	4K x 1	CMOS/epi (fast)	FUJ	~100							UCB	

Test Org.*	Device	Function	Technology	Mfr.	Effective SEU LET* Threshold	Device Xsection (cm^2)	Bits Tested	Bit Xsection (cm^2)	Test Date	LUth	LU Xsection (cm^2)	Fac.	Remarks 31-Aug-99
	Note: Entries in **RED** indicate data added since the 1997 Compendium.												
NTT	MB8404	4K x 1	CMOS bulk	FUJ	<<18	8.0E-03		2.0E-06				TU	Tested at Toyko University.
ARSP	MB84256	32K x 8	CMOS	FUJ	<3	1.0E+00			Nov-89	25	6.0E-05	UCB	
ESA	MB84256	32K x 8	CMOS (1.8 µm)	FUJ	2			2.4E-07	Dec-91			IPN	Adams, et al, 91IEEE TNS, No. 6, pg 1686.
ARSP	MBM10474A	SRAM	Bipolar/ECL	FUJ	<<3	3 E-2		7.3E-06		>40		UCB	Koga, et. al., 95IEEE TNS, No. 6, pg 1823. D/C 8802.
ARSP	MCM6226	128K x 8	CMOS/NMOS	MOT	<3	2.0E-01			Oct-92	45	2.0E-05	UCB	
MMS	**MCM6246WJ20**	**512K x 8**	**CMOS/epi, 0.5µm feat., Rev W51**	**MOT**	**~1**			**1.0E-07**	**1997**			**CYC**	**Poivey, et al, 98IEEE Wrkshp Rec., pg 68. D/C 9602**
ARSP	MDC5114	1K x 4	CMOS/epi	MED	50							UCB	
CNES	MHS65162	2K x 8	CMOS/epi	MHS					Feb-90	>72		IPN	Same technology as HM65252
ESA	MHS65162	2K x 8	CMOS/epi	MHS		1.2E-02		7.0E-07	1993	>20		GSI	Metzger et al, RADECS 93. Device and bit cross sections @ LET = 20.
ESA	MHS65162	2K x 8	CMOS/epi (10 µm)	MHS	4	3.0E-02			1993			GSI	Dreute, RADECS 91 & 93. X-section @ LET = 35. High vs low energy comp.
ESA	MHS65664	8K x 8	CMOS/epi (5 µm)	MHS	<10	1.2E-02			1993	>35		GSI	Dreute et al, RADECS 93
JPL/ARSP	MM54C200D	256 x 1	CMOS	NSC	>120							UCB	
JPL/ARSP	MM54C929	1K x 1	CMOS	NSC	15	1.0E-02		1.0E-06				UCB	Latchup
ARSP	MSC810	1K	CMOS	NSC	16	3.0E-03		3.0E-06				UCB	Latchup
NTT	MSM5164	64K	CMOS	MIT	3.5	1.0E-01		1.5E-06				TU	Latchup. Tested at Toyko University.
NTT	MSM5164	64K	CMOS/epi	MIT						<18	1.3E-03	TU	Note latchup of CMOS/epi technology
MMS	MSM8128	128K x 8	CMOS	HTC					1994			GANIL	Poivey, et al, 94IEEE TNS, No. 6, pg 2295. SHE (Single Hard Error), @ LET >50, 1.0E-3 cm2,
JPL	MSM8128K	128K x 8	CMOS	MOC	2.8	4.0E-03			Dec-93	26		BNL	Cross section at LET = 26.
JPL	MSM8128KL	128K x 8	CMOS	MOC	2.8	4.0E-03			Dec-93	26		BNL	No differences in -K and -KL devices. Cross section at LET = 26.
ARSP	MSM8128SLMB	128K x 8	CMOS	MIT	4	1.0E+00			May-90	85	4.0E-06	UCB	
ARSP	MSM8128SLMB-10	128K x 8	Hitachi dies	MOC	~4	1.0E+00			May-90	72	3.0E-06	UCB	Koga. Compare to Hitachi data. Proton data exists. Stuck bit Xsection <1E-7 cm^2.
CNES	MT5C1001	1M x 1	CMOS	MCN	<0.3	5.0E-01		4.0E-07 - 7.0E-07	1993			IPN	Duzellier, et al, 93IEEE Wrkshp Rec, pg 36. D/C 9133. Bit cross section is pattern dependent. Proton data exists.
MMS	MT5C1008	128K x 8	CMOS	MCN					1994			GANIL	Poivey, et al, 94IEEE TNS, No. 6, pg 2295. SHE (Single Hard Error), @ LET >50, 1.0E-3 cm2.
CERT	MT5C1008	128K x 8	CMOS	MCN	0.6	1.0E+00			1991			IPN	Duzellier, et al, 95IEEE TNS, No. 6, pg 1797. All "1s" worst case; includes multiple errors. High vs medium energy beam study. Comparison studies done at Saturne
CNES	MT5C1008	128K x 8	CMOS/epi (7 µm)	MCN	~2	6.0E-01			May-91	>26		IPN	All "1s" is worst case; includes multiple errors. Tested before May 91.
CNES	MT5C1008	128K x 8	CMOS	MCN	<1.7	1.8E+00		2.5E-07 - 2.5E-06	1993			IPN	Ecoffet et al, 93IEEE & 92IEEE Wrkshp Rec.s. D/C 9125. Bit cross section is pattern dependent. Proton data exists.
CNES	MT5C1008	128K x 8	CMOS/epi	MCN	5	2.0E+00			Aug-91			IPN	D/C 9101. All '1s" is worst case.

Heavy Ion SEE

Test Org.*	Device	Function	Technology	Mfr.	Effective SEU LET* Threshold	Device Xsection (cm^2)	Bits Tested	Bit Xsection (cm^2)	Test Date	LUth	LU Xsection (cm^2)	Fac.	Remarks 31-Aug-99
	Note: Entries in **RED** indicate data added since the 1997 Compendium.												
CNES	MT5C1008	128K x 8	CMOS/epi LCRP	MCN	<1.7	2.0E-03		2.9E-09	1992			IPN	Duzellier, et al, 93IEEE TNS, No. 6, pg 1797. Bit X-section w/checkerboard. LCRP = Low current reistor process. Comparison tests at Saturne (France)
ARSP	MT5C1008	128K x 8	CMOS/epi	MCN	4	2.0E-02			Jul-91	>100		UCB	Koga, et al, 91IEEE-TNS, No. 6, pg 1529. Low current device cross section = 1.0E-02.
ARSP	MT5C1008	128K x 8	CMOS/epi LCRP?	MCN	4	2.0E-03			1993	>100		UCB	Koga, et al, 93IEEE TNS, No. 6, pg 1941. Single word multiple upsets (SMUs). Low cross section implies low current devices.
CERT/ CNES	MT5C1008	SRAM	CMOS	MCN	0.6	1.0E+00							
CERT/ CNES	MT5C1008	SRAM	CMOS/epi LCRP process	MCN	<1.7	2.0E-03							
JPL	MT5C1008C	128K x 8	CMOS/epi LCRP?	MCN	<3	2.0E-02			Sep-91	>110		UCB	Hard errors annealed @ RT after test.
MMS	MT5C1008C	128K x 8	CMOS/bulk	MCN					1994	75	4.0E-04	GANIL	Dufour 92IEEE TNS; Poivey 94IEEE TNS; Beaucour 93IEEE Wrkshp Rec.. Hard errors.
MMS	MT5C1008CW	128K x 8	CMOS/bulk	MCN					1992	75	4.0E-04	GANIL	Dufour, et al, 92IEEE Wrkshp Rec., pg 21..
CNES	MT5C1009	128K x 8	Date Code "ES"	MCN	<1.7			1.0E-10 - 1.2E-08	1993			IPN	Duzellier, et al, 93IEEE Wrkshp Rec., pg 36. D/C ES. Bit X-section pattern dependent.
LIN	MT5C1608	2K x 8	CMOS	MCN					Apr-91	27		BNL	
LIN	MT5C1608	2K x 8		MCN	<1.4				Aug-90	<26		BNL	
ARSP	MT5C256	32K x 8	CMOS/NMOS	MCN	~3	1.0E+00			Jun-92	>100		UCB	Cross section is a factor of 100 smaller for high resistance
LIN	MT5C2568	32K x 8	CMOS/epi	MCN					1989	<40		UCB	Kinnison
LIN	MT5C2568	32K x 8	CMOS bulk	MCN					1991	>164		UCB	Sferrino '91.
ARSP/LIN	MT5C2568	32K x 8	CMOS/NMOS	MCN	<1.4	6.0E-01			Dec-88	15	1.0E-05	UCB	Includes multiple errors. Also tested at BNL (8/90) with same results.
ARSP	MT5C2568	32K x 8	CMOS/epi NMOS	MCN	3	9.0E-01			Jul-91	>100		UCB	Includes multiple errors.
JPL	MT5C2568	32K x 8	CMOS/epi (0.65 µm feature)	MCN	<1.4	6.0E-02			Dec-93	>72		BNL	
JPL	MT5C2568-35	32K x 8	CMOS/epi	MCN	<1.4	3.0E-02			Dec-93	>72		BNL	D/C 9333. Later S12 process. Same as following except no giant error clusters. All "1s" worst case.
JPL	MT5C2568-35	SRAM	CMOS/epi	MCN	<1.4	3.0E-02			Dec-93				
JPL	MT5C2568-70	32K x 8	CMOS/epi	MCN	<1.4	3.0E-02			Dec-93			BNL	D/C 9237. Earlier S06 process. Giant 32K error clusters at LET > 26. All "1s worst case.
JPL	MT5C2568-70	SRAM	CMOS/epi	MCN	<1.4	3.0E-02			Dec-96				
ESA	MT5C2568C	32K x 8	CMOS	MCN	<1.7			1.5E-06	1993	>40		IPN	Harboe-Sorensen, RADECS 93, pg 490. See later technology.
CERT	MT5C2568C	32K x 8		MCN	1	3.5E-01			1991	>72		IPN	Falguere, RADECS 91, pg 479.
MMS	MT5C2568C	32K x 8	CMOS 2M-2P	MCN	<1.0	6.0E-01			1992	23	1.0E-02		Dufour, et al, 92IEEE Wrkshp Rec., pg 21.. Includes multiple errors.
JPL	MT5C2568C-35	SRAM	S12 process (0.65 µm.)	MCN	<1.45	1.0E-02			Apr-96				
ARSP	MWS5501	1K	CMOS/SOS	RCA	>120							UCB	
JPL/ARSP	NBRC4042	16K	CMOS	HUG	20	2.0E-03		1.2E-07				UCB	

Heavy Ion SEE

Test Org.*	Device	Function	Technology	Mfr.	Effective SEU LET* Threshold	Device Xsection (cm^2)	Bits Tested	Bit Xsection (cm^2)	Test Date	LUth	LU Xsection (cm^2)	Fac.	Remarks 31-Aug-99
	Note: Entries in **RED** indicate data added since the 1997 Compendium.												
ARSP	OW5962	32K x 8	CMOS	OWI	8	5.0E-02			Jul-89	22	3.0E-03	UCB	Sony die
ARSP	OW62256	32K x 8	NMOS/CMOS	OWI	5	4.0E-01			Dec-87	>80		UCB	Includes multiple errors. HTC die
ARSP	OW62256CD	32K x 8 (die)	CMOS	HTC					May-90	>80		UCB	Koga
JH	P4C163	8K x 9	CMOS	PFS					Jan-91	30		BNL	
ARSP	P4C164L	8K x 8	CMOS	PFS					Sep-89	8	1.0E-02	UCB	
ARSP	P4C188L	16K x 4	CMOS	PFS	5	2.0E-02			Sep-89	11	8.0E-03	UCB	
ARSP	PACE422	256 x 4	Adv. CMOS	PFS	~1				Jun-87	10	2.0E-03	UCB	
JPL	PDM41256SA250	SRAM	NSC die	PDM	3.4				Apr-96	12	3.0E-06	BNL	LU masks SEU threshold.
JPL/ARSP	SA3001	2K x 8	CMOS	SNL	>75							UCB	
ARSP	SA3115	16K	CMOS	SNL	>70							UCB	
ARSP	SA3240	16K	CMOS	SNL	>250							ORNL	
MMS	SMJ44C251	256K x 4	CMOS (1 µm)	TIX	0.5			1.2E-06	Jul-93	>46		GANIL	Beaucour, 93IEEE Wrkshp Rec., pg 20.
ARSP	SSM7188	16K x 4	BiCMOS	SRT					Jun-88	>60		UCB	
ARSP	TA11370	16K	CMOS/SOS	RCA	>50							UCB	For Vcc = 5.0 V. Note bias-dependent threshold.
ARSP	TA11370	16K	CMOS/SOS	RCA	>80							UCB	For Vcc = 10 V. Note bias-dependent threshold.
ARSP	TA12702	16K	CMOS/SOS	RCA	>70							UCB	
ARSP	TA13316	16K	CMOS/SOS	RCA	>80							UCB	
ARSP	TA597	1K	CMOS	SNL	>70							UCB	
SNL	**TA786**	**16K test vehicle**	**CMOS, 0.5µm, rad-tolerant.**	**SNL**	**~8**	**3.0E-03**			**1997**			**BNL**	**Dodd, et al, 98IEEE TNS, Vol. 45, No. 6, pg 2483.**
ESA	TC5516	2K x 8	CMOS	TOS	~6			3.0E-06	Dec-90	<27	1.0E-04	IPN	
JPL	TCC244 (Rad Hard)	256 x 4	CMOS	RCA	>100							UCB	
JPL/ROCK	TCC244 (SA3938)	256 x 4	CMOS CCL	SNL	>75							UCB	
JPL/ARSP	TCS130S	16K	CMOS/SOS	RCA	~48							UCB	Commercial part
ARSP	TCS146	4K	CMOS/SOS	RCA	>30	4.0E-04		1.0E-07				UCB	
ARSP	TCS205H	4K	CMOS/SOS	RCA	~120							UCB	
ARSP	TCS210S	4K	CMS/SOS	RCA	37	3.0E-04		8.0E-08				UCB	
CNES	TMS	16K	HCMOS3/epi	TMS	6	4.0E-02			Nov-90	>54		IPN	Chapuis. ESA Conference Nov 90.

Test Org.*	Device	Function	Technology	Mfr.	Effective SEU LET* Threshold	Device Xsection (cm^2)	Bits Tested	Bit Xsection (cm^2)	Test Date	LUth	LU Xsection (cm^2)	Fac.	Remarks 31-Aug-99
	Note: Entries in **RED** indicate data added since the 1997 Compendium.												
CNES	TS4H6408	8K x 8	SOI	TMS	>114				1992			IPN	Ecoffet preprint. D/C 9151.
HAR	TSOS4	64K x 1	Std. Cell Lib. RH CMOS/SOS	HAR	>138				Oct-91			BNL	W. Newman, Harris memo
ROCK	UT67164	8K x 8	CMOS "prototype flow"	UTM	>37				Jul-93	>37		BNL	Ferdon. D/C 9320.
JPL	V1608	2K x 8	CMOS	VTC	15	2.0E-02		1.0E-06	Feb-87			BNL	
ARSP	XCDM62256	32K x 8	NMOS/CMOS	RCA	3	4.0E-01			Dec-87	30	1.0E-03	UCB	Includes multiple errors.
ARSP	XTA11246Z		CMOS/SOS	RCA	50							UCB	
		Flash Memories											
JPL	**28F016SA**	**2M x 8 or 16M x 1 NOR**	**ETOX process**	**INT**	**7**	**1E-06 to 1E-07**			**Nov-95**	**44**	**1.0E-04**	**BNL**	**Schwartz, et al, 97IEEE TNS, No. 6, pg 2315. D/C 96??. Functional errors.**
JPL	**28F016SV**	**2M x 8 or 16M x 1 NOR**	**ETOX process**	**INT**	**7**	**1E-06 to 1E-07**			**Nov-95**	**44**	**1.0E-04**	**BNL**	**Schwartz, et al, 97IEEE TNS, No. 6, pg 2315. D/C 9524 & 9534. Functional errors.**
JSC	DPZ128x16A3	128K x 16	Two 128Kx8 dice	HTC					May-93	20			
JPL	**KM29N16000**	**2M x 8 NAND**	**CMOS**	**SAM**	**11**	**2.0E-04**	**4000**		**Mar-97**	**~60**		**BNL**	**Schwartz, et al, 97IEEE TNS, No. 6, pg 2315. D/C 9530. Stuck bits at LET = 37. All observed upsets probably in peripherals.**
JPL	**KM29N32000**	**4M x 8 NAND**	**CMOS**	**SAM**			**64000**						**Schwartz, et al, 97IEEE TNS, No. 6, pg 2315. D/C 96?? No stuck bits.**
		DRAMs											
NRL	4164	64K x 1	NMOS	INT									
IBM	44400	1M x 4	CMOS	TIX					1990		2.0E-06		
ESA	44400	1M x 4	CMOS Rev B design (shrink)	TIX	1.5	2.0E+00		5.0E-07		>165			TIX in Japan
JPL	**µPD4265165**	**4M x 16**	**CMOS (3.3 V)**	**NEC**	**<1.7**			**2.0E-09**	**1998**			**BNL TAM**	**Swift, RADECS98 preprint. D/C 9738KE006**
GSFC	**0116400J1C-70 rev C**	**4M x 4**	**CMOS**	**IBM**	**3**	**7.0E-02**			**Dec-96**	**50**	**2.0E-04**	**UCB**	**LaBel, et al, 96IEEE Wrkshp Rec., pg 19. Cell errors.**
GSFC	**0116400J1C-70 rev C**	**4M x 4**	**CMOS**	**IBM**	**5**	**7.0E-02**			**Dec-96**	**50**	**2.0E-04**	**UCB**	**LaBel, et al, 96IEEE Wrkshp Rec., pg 19. Block errors.**
GSFC	**0116400J1D**	**4M x 4**	**CMOS**	**IBM**	**<3.38**				**1996**	**>11.5**		**UCB TAM**	**LaBel, et al, 97IEEE Wrkshp Rec., pg 14. Bit errors.**
GSFC	**0116400J1D**	**4M x 4**	**CMOS**	**IBM**	**3.9**				**1996**	**>11.5**		**UCB TAM**	**LaBel, et al, 97IEEE Wrkshp Rec., pg 14. Bit and block errors.**
ESA	**0117400BT1F-60**	**4M x 4 (3.3 V)**	**CMOS (IBM - ES4)**	**IBM**	**~1**			**4.0E-08**	**1997**			**CYC**	**Harboe-Sorensen, et al, 98IEEE Wrkshp Rec., pg 74.**
CNES	01G9274		CMOS	IBM	2.5			2.4	1993				D/C ES.
SEI	**14C0164RP**	**4M x 4**	**CMOS**	**HTC**	**4.5**	**3.0E-01**			**Jan-97**	**>89**		**UCB TAM**	**Layton, et al, 98IEEE Wrkshp Rec., pg 170.**
ARSP	2164A	64K x 1	NMOS	INT	~1	2.0E-01		300	Dec-89				
ESA	44100DM-80	16K x 1	CMOS(EPIC) 0.75 µm line width	TIX	1.5	2.0E+00		50	1993	>165			
ESA	D424100V-80	4M x 1	CMOS	NEC	~1			0	1991	>50			

Heavy Ion SEE

Test Org.*	Device	Function	Technology	Mfr.	Effective SEU LET* Threshold	Device Xsection (cm^2)	Bits Tested	Bit Xsection (cm^2)	Test Date	LUth	LU Xsection (cm^2)	Fac.	Remarks 31-Aug-99
	Note: Entries in **RED** indicate data added since the 1997 Compendium.												
JPL	**D426S165G5**	**4M x 16 EDO (3.3 V)**	**CMOS**	**NEC**	**~1**			**1.0E-07**	**1998**			**BNL**	**Swift, RADECS98 preprint. D/C 9738KE006**
ROCK	EDI 41024C100QB	1M x 1		EDI	1.4	1.1E-01		10	Apr-92	>82			
ESA	HM514100ZP8	4M x 1	CMOS	HTC	~2			12	Sep-91	>40			
JPL	**HM5165165AJ**	**4M x 16 EDO**	**CMOS**	**HTC**	**<20**			**1.0E-06**	**1998**			**BNL**	**Swift, RADECS98 preprint. D/C 9737**
ESA	**HM51W16100B**	**CMOS**	**CMOS**	**HTC**	**~1**			**8**	**1997**			**CYC**	**Harboe-Sorensen, et al, 98IEEE Wrkshp Rec., pg 74.**
ESA	HYB514100J-10	4M x 1	CMOS (n-well)	SIE	~1			6.0E-07	Sep-91	>40			
JPL	IS256		NMOS	MCN	1	6.0E-01		2.4E-06	Aug-87		1.0E-04		
JPL	IS256 (with EDAC)		NMOS	MCN	<2	1.0E-02			Aug-87				
ESA	KM41C16000J	16M x 1	CMOS	SAM	<1			2.0E-07	1995	>110			
ESA	KM41C4000Z-8	4M x 1	CMOS	SAM	~2			4.0E-07	Sep-91	>40			
GSFC	KM44C4000AJ-7	4M x 1	CMOS	SAM	<1.46	3.0E+00		1.7E-07	Jul-94	>110			
ESA	KM44C4000J-6	4M x 1	CMOS	SAM	<1			2.0E-07	1995	>110			
ICI	**KM44S16030CT-GL**	**16M x 4 (3.3 V)**	**CMOS**	**SAM**	**~20**	**~2.5E+01**			**1998**	**>50**			**Henson, et al, 99IEEE Wrkshp Rec. Preprint (paper W-7). Static mode. Multiple upsets and stuck bits seen at high LETs.**
ICI	**KM44S16030CT-GL**	**16M x 4 (3.3 V)**	**CMOS**	**SAM**	**~20**	**~1.0E+01**			**1998**	**>50**			**Henson, et al, 99IEEE Wrkshp Rec. Preprint (paper W-7). Dynamic mode. Multiple upsets and stuck bits seen at high LETs.**
ICI	**KM44S32030CT-GL**	**32M x 4 (3.3 V)**	**CMOS**	**SAM**	**~15**	**~4.0E+01**			**1998**	**>82**			**Henson, et al, 99IEEE Wrkshp Rec. Preprint (paper W-7). Dynamic and static modes.**
ESA	**KM44V4100AJ**	**4M x 4 (3.3 V)**	**CMOS**	**SAM**	**~1**			**5.0E-08**	**1997**			**CYC**	**Harboe-Sorensen, et al, 98IEEE Wrkshp Rec., pg 74.**
JPL	KM48V8004AK-6	DRAM	CMOS	SAM					Mar-97	56±4	1.3E-06		
JPL	**KM48V8104AS-6**	**8M x 8 EDO**	**CMOS**	**SAM**	**~1**			**2.0E-08**					
CNES/ ALC	LUNA-C	4M x 4	CMOS/epi with ECC-- off or on	IBM	~3	~2.0E-01			1994	>120			
CNES/ ALC	LUNA-C	4M x 4	CMOS/epi with ECC-- off or on	IBM	~3	3.0E-03			1994	>120			
JPL/LFS	LUNA-C DD3	4M x 4	CMOS/epi with ECC-- off	IBM	4			2.0E-08	Aug-94	>120			
CNES/ ALC	LUNA-E	4M x 4	CMOS/epi without ECC	IBM	~3	1.0E-01			1994	>120			
GSFC	LUNA-ES2	4M x 4	CMOS/epi without ECC	IBM	<3.4				Mar-97	11.5	1.0E-04		
JPL	M41256	256K x 1	NMOS	ATT	<2	5.0E-01		2.0E-06					
ARSP	M5M44100	4M x 1	CMOS	MIT	<3.3	1.0E+00			Dec-94	>60			
JPL	M5M467800AJ	64M	CMOS	MIT					Mar-97	~82	1.2E-06	BNL	LU X-section still unsaturated @ LET = 82. Parts were only partially operational.
ESA	MB8116100-60PJ "F"	16M x 1	CMOS	FUJ	<1			1.0E-07 - 2.0E-07	1995	>110		BNL	Harboe-Sorensen, 95IEEE Wrkshp Rec., pg 42. Row errors noted. Comparison testing done at UCL (Belgium)
GSFC	MB8116400-60PJ	16M x 1	CMOS	FUJ	<1.4	3.5E+00			May-94	>80		BNL	SEFI @ LET ~50. LaBel test
GSFC	MB8116400-60PJ	DRAM	CMOS	FUJ	<1.4	3.0E+00			Dec-96	80		BNL	LaBel, et al, 96IEEE TNS, No. 6, pg 2974. SEFI @ LET = 50. D/C 9337. Vcc = 5V.

Heavy Ion SEE

Test Org.*	Device	Function	Technology	Mfr.	Effective SEU LET* Threshold	Device Xsection (cm^2)	Bits Tested	Bit Xsection (cm^2)	Test Date	LUth	LU Xsection (cm^2)	Fac.	Remarks 31-Aug-99
	Note: Entries in **RED** indicate data added since the 1997 Compendium.												
JPL/ARSP	MB81256	256K x 1	NMOS	FUJ	~2	1.0E-01		4.0E-07				BNL	
ESA	MB814100-10PSZ	4M x 1	CMOS	FUJ	~1			8.0E-07	Sep-91	>50		IPN	RADECS 91
ROCK	MCM6605A	4K	NMOS	MOT	~14	2.0E-02		5.0E-06				UCB	
ROCK	MDM11000TMB	1M x 1	CMOS	NEC	<0.5	2.4E-01		2.4E-07	Apr-92	25	1.0E-04	BNL	Dynamic test - MOSAID MS2200 Memory tester. Fabbed at Mosaic.
ROCK	MDM14000G	4M x 1	CMOS	HTC	1.7	1.2E-01		3.0E-08	Apr-92	>82		BNL	MOSAID MS2200 Memory tester. Fabbed at Mosaic.
JPL	MDM14000GMB-80	4M x 1	CMOS-- MIT M5M44100 die	MIT					Nov-95	>87		TAM	Mosaic package. No observed stuck bits.
ESA	MKB4116	16K x 1	NMOS	MOS					Dec-91				C. S. Dyer, J. Stephen refer to calc'd SEU rate in 91IEEE TNS, No. 6, pg 1700.
JPL	MT1259	256K x 1	NMOS	MCN	<1				Dec-89			BNL	Upsets depend on bias. See 88IEEE TNS, No. 6, pg. 1644 & 89IEEE TNS, No. 6, pg. 2267.
CNES	MT4C1004C	4M x 1	CMOS/epi (0.8 µm. line width)	MCN					Jan-92	>54		IPN	Ecoffet, CNES report RA/DP/QA/CE/92-513 on Test Campaigns 8&9. D/C 9109.
ESA	MT4C1004C	4M x 1	CMOS (0.8 µm. line width)	MCN	~1.5			3.0E-07 - 8.0E-07	1991	>120		BNL & IPN	Harboe-Sorensen, RADECS 91, & 93, pg 490. D/C 2C9236C.
ARSP	MT4C4001	1M x 4	CMOS/epi (7 µm)	MCN	~3	2.0E+00			Mar-92	>100		UCB	At 70 deg. C. LU_{th} >100 at R.T.
CNES	MT4C4001	1M x 4	CMOS/epi	MCN	<0.4 to <1.7	1.0E+00		5.0E-07 - 1.5E-06	1993			IPN	Duzellier, et al, 95IEEE TNS, No. 6, pg 1797. D/C 9109 & 9248. High vs medium energy beam study. Comparison studies done at Saturne (France)
ESA	MT4C4001JC	1M x 4	engr sample-shrunk 0.6µm	lMCN	~1.5			4.0E-07 - 8.0E-07	1993	>120		IPN	Harboe-Sorensen, RADECS 93, pg 490. D/C 9244. Process D15B.
GSFC	MT4C4M4B1DW	4M x 4	CMOS	MCN	<1.4				May-94	12 to 26		BNL	LaBel. LU obscures LET_{th}.
ESA	MT4C4M4B1DW	4M x 4	CMOS	MCN	<1			1.0E-07	1995	53		BNL	Harboe-Sorensen, 95IEEE Wrkshp Rec.,pg 42. Row errors =2E-4 cm2. D/C 9406B.
GSFC	MT4C4M4B1DW	4M x 4	CMOS	MCN	<1.4	2.0E-01			Dec-96	12 to 26	2.0E-04	BNL	LaBel, et al, 96IEEE TNS, No. 6, pg 2974. D/C 9404. Vcc=5V.
ESA	**MT4LC4M4D42 Rev T**	**4M x 4 (3.3 V)**	**CMOS**	**MCN**	**~1**			**6.0E-08**	**1997**			**CYC**	**Harboe-Sorensen, et al, 98IEEE Wrkshp Rec., pg 74.**
IBM	SMJ27C128-25	16K x 8	CMOS	TIX					May-93			BNL	The data here was taken as a subset of the TIX SM320E15 DSP.
IBM	SMJ416400-1 thru-6	4K x 4	CMOS epi?	TIX	0.4			1.1E-08	Jan-93	>70		BNL	Functional interrupt LET(th) = 12; 2.7E-06 cm^2. WP-2 (Jim Pollack)
CERT/ CNES	SMJ416400-Rev. B	DRAM	CMOS/epi (0.5 µm)	TIX	~5	5.0E+00						IPN	Duzellier, et al, 95IEEE TNS, No. 6, pg 1797. All "1s" @ high energy. High vs medium energy beam study. Comparison studies done at Saturne (France)
CNES	SMJ44100	4M x 1	CMOS/epi	TIX	<0.4			>2.4E-07	1992			IPN	Duzellier, et al, 93IEEE Wrkshp Rec. pg. 36. D/C ES. Proton data exists. See following entry.
IBM	SMJ44400	1M x 4	CMOS epi?	IBM					1990	16		BNL	Soft error data exists.
GSFC	TC5117400FT-70	4M x 4	CMOS	TOS					May-94			BNL	Pending analysis. LaBel
GSFC	TC5117400J-6	4M x 4	CMOS	TOS	<1.46	3.0E+00		1.8E-07		>100		BNL	LaBel, et al, 96IEEE TNS, No. 6, pg 2974. SEU cross section @ LET = 100. No stuck bits. No multiple errors. Vcc=5V. D/C YB4927
ESA	TC514100Z-10	4M x 4	CMOS	TOS	~1			6.0E-07	Sep-91	>50		IPN	RADECS 91
JPL	**TC5165805AFT-50**	**8M x 8**	**CMOS**	**TOS**	**~1**	**1.0E-08**			**1998**			**BNL**	**Swift, RADECS98 preprint. D/C 9721. Cross section without row or column upsets.**
WU	TC51832p	DRAM	planar cell structure [cap & Xtr]	TOS	~2				Jul-96			WU	Matsukawa preprint. Data from He ion microprobe , IEEE, July 1996
GSFC	TMS416400	DRAM	CMOS	TIX	~2				Mar-97			BNL?	LaBel, et al, EEE Links, Vol. 3, No. 1, Mar 97, pg 5

Test Org.*	Device	Function	Technology	Mfr.	Effective SEU LET* Threshold	Device Xsection (cm^2)	Bits Tested	Bit Xsection (cm^2)	Test Date	LUth	LU Xsection (cm^2)	Fac.	Remarks 31-Aug-99
	Note: Entries in **RED** indicate data added since the 1997 Compendium.												
ESA	TMS416400A (1992)	16M x 1	CMOS	TIX	<1		15		1995	>75	1.0E-04	BNL	Harboe-Sorensen, 95IEEE Wrkshp Rec., p 42. Row errors =1.0E-04 cm2/device. Strong preference for 1 to 0 transitions.
GSFC	TMS416400DJ-60	4M x 4	CMOS	TIX	3				Mar-97			BNL?	LaBel, et al, EEE Links, Vol. 3, No. 1, Mar 97, pg 5
GSFC	**TMS416400DJ-60**	**4M x 4**	**CMOS**	**TIX**	**<2.5**				**1996**	**>65**		**BNL**	**LaBel, et al, 97IEEE Wrkshp Rec., pg 14. Bit errors.**
CNES/ ALC	TMS416400-Rev. B	DRAM	CMOS/epi (0.5 µ)	TIX	<<1.7	5.0E+00				>57		BNL IPN	Calvel, 94IEEE TNS, No. 6, pg 2267. Loss of functionality @ LET = 25; 5.0E-05 cm^2. Full row error cross section = 1.0E-04 cm^2. Also half row errors.
ESA	TMS4416	16K x 4	NMOS	TIX	<5			2.0E-06	Dec-90			IPN	Harboe-Sorensen, et al, 90IEEE TNS, No. 6, pg. 1938.
		Non-Volatile RAMs											
J	FMx1208	512 x 8	CMOS/epi	RMT	~11	3.0E-03			Jun-92	45		BNL	Ferroelectric RAM (dynamic test)
J	FMx1408	2K x 8	CMOS	RMT	<<30	2.0E-04			Jun-92	<<30		Cf-252	1.0E-06 cm^2 (Dyn) & 4.0E-06 cm^2 (non-vol). Ferroelectric RAM (dynamic test)
CNES	P10C68	8K x 8	CMOS/SNOS	PLS	7	3.5E-01			1992			IPN	SRAM configuration
CNES	P10C68	8K x 8	CMOS/SNOS	PLS	114				1992			IPN	EEPROM configuration
		PROMs											
JPL	93451	(Fusible link)	Bipolar STTL	FAS	>37				Jan-88	>104		BNL	Corrects prior data.
JPL	2764A	8K x 8	NMOS	INT	<17	1.5E-03				>120		BNL	
JPL/ARSP	27C64	8K x 8	CMOS	INT					Mar-88	14	1.0E-04	BNL	Also tested @ UCB.
MMS	82HS641	8K x 8	Bipolar	SGN	31	7.0E-06			1992	>32		GANIL	Dufour, et al, 92IEEE Wrkshp Rec., pg 21.
GSFC	82HS641A	8K x 8	Bipolar	SGN	>73				Dec-91	>73		BNL	Compare to GANIL data above.
ARSP	AM27S49A	8K x 8	Bipolar TTL	AMD	7	9.0E-05			Dec-89			UCB	No permanent errors. Errors for read cycle only.
BREL	CY7C261	8K x 8	CMOS	CYP	<15				1995	<15	7.0E-04	UCB?	Normand et al, 95IEEE Wrkshp Rec., pg. 33.
MMS	CY7C261-55	8K x 8	CMOS	CYP	<32	2.0E-01			1992	<32	5.0E-04	GANIL	Dufour, et al, 92IEEE Wrkshp Rec., pg 21.
JPL	HM6611	32 x 32	CMOS	HAR					1983	45	1.0E-04	UCB	Soliman & Nichols, 83IEEE TNS, No. 6, pg 4514.
JPL	HM6616	2K x 8	CMOS/epi (12 µm)	HAR	<37	1.0E-02			May-87	40		UCB	
JPL/CNES	HM6617	2K x 8	CMOS/epi (7 µm)	HAR	12	7.0E-05			Dec-87				
GD	HM6617	2K x 8	CMOS/epi	HAR		3.0E-06			Nov-87			Cf-252	Output buffer upsets.
MMS	HM6617	2K x 8	CMOS	HAR	32	3.0E-04			1992	58	2.0E-04	GANIL	Dufour, et al, 92IEEE Wrkshp Rec., pg 21.
JPL/HAR/ ARSP	HM6641	512 x 8	CMOS	HAR	22				1983	42	1.0E-04	UCB	Soliman & Nichols, 83IEEE TNS, No. 6, pg 4514.
JPL	HS1-6617RH-8	2K x 8	CMOS/epi	HAR	19	2.0E-05			Oct-90	>120			Address register upsets only. Compare to HM6617.
	HS6616 (rad hard)	2K x 8	CMOS/epi	HAR					Jun-87	>120			At T=120 deg. C.

Test Org.*	Device	Function	Technology	Mfr.	Effective SEU LET* Threshold	Device Xsection (cm^2)	Bits Tested	Bit Xsection (cm^2)	Test Date	LUth	LU Xsection (cm^2)	Fac.	Remarks 31-Aug-99
	Note: Entries in **RED** indicate data added since the 1997 Compendium.												
MMS	HS-6664RH	8K x 8	CMOS, TSOS-4 process	HAR	116				1994	>116		BNL	Au at 45 deg angle. Harris Space Product News, 3rd Q, 1994
JPL	MB7144E	8K x 8	Bipolar	FUJ					1992	>140		GANIL	Dufour, et al, 92IEEE Wrkshp Rec., pg 21.
ROCK	R29791	8K x 8	Bipolar	RAY	15	2.4E-05			Apr-93	>74		BNL	Upsets are transients at output; no lost data.
MMS	R29793	8K x 8	Bipolar	RAY	8	3.0E-05			1992	>87		GANIL	Dufour, et al, 92IEEE Wrkshp Rec., pg 21.. Peripherals only.
LIN	R29793	8K x 8	Bipolar Fuse link	RAY					1991	>164		BNL	Sferrino '91
UTMC	UT28F64	8K x 8 (antifuse-based)	CMOS	UTM					Jul-96	>128			Anthony Jordan, UTMC News
JPL	**XQ1701L**	**1M x 1**	**Bulk CMOS**	**XIL**	**8**	**1.5E-05 - 3.0E-05**			**1999**	**55**	**1.0E-05**	**BNL**	**Guertin, et al, 99IEEE Wrkshp Rec. Preprint. End-of-Pass, address and SEFI errors.**
		EAPROMs											
ROCK	3022	1K	MNOS/SOS	ROC	<37							UCB	Permanent damage seen in the Read mode using 150MeV Kr.
ROCK	6030	1K	MNOS	WEC	>37							UCB	
ROCK	ER3400	4K	MNOS	GIC	<37							UCB	Permanent damage seen in the High Field mode. OK in Read mode
ROCK	NCR3400	4K	MNOS	NCR	<37							Cf-252	Also UCB data. Permanent damage seen in the High Field mode. OK in Read mode
ROCK	SA2475	256	MNOS	SNL	>37							UCB	
ROCK	SA2998	1K	MNOS	SNL	<37							Cf-252	Permanent damage seen in the High Field mode. OK in Read mode
ROCK	SA2999	16K	MNOS	SNL	<37							Cf-252	Permanent damage seen in the High Field mode. OK in Read mode
		EEPROMs											
MMS	28C010	128K x 8	CMOS bulk (FLOTEX)	SEQ	4 to 10	1.0E-04			1994	32	5.0E-05	GANIL	Poivey, et al, 94IEEE Wrkshp Rec, pg. 20. D/C 9330. Hard errors @ LET = 16. SEGR?
ESA	28C010D-20	128K x 8	CMOS	XIC	<1.5	>5.0E0-5			Jan-96			BNL	D/C 9236."Write" mode. Low LETs only. Harboe-Sorensen, Ibid. above
GSFC	**28C010TE**	**128K x 8**	**CMOS**	**HTC**	**>69**				**1997**	**>69**		**BNL**	**O'Bryan, et al, 98IEEE Wrkshp Rec., pg 39. Static mode testing.**
GSFC	**28C010TE**	**128K x 8**	**CMOS**	**HTC**	**~20**				**1997**	**>69**		**BNL**	**O'Bryan, et al, 98IEEE Wrkshp Rec., pg 39. Programming mode testing. Byte errors @ LET ~20: Block errors ~25: Stuck bits ~59.7.**
ESA	28C1024		CMOS	ATM	<11	4.0E-05						BNL	Transients, word & block errors too.
JPL	28C256	32K x 8	CMOS	ATM	3				Jan-94			BNL	For "read errors. Stuck bits (write) @ LET>60. Stop/start runaways @LET >16.
JH/LIN	28C256	32K x 8	CMOS/epi	SEQ					Apr-90	>164			Errors of an entire byte occur during "write" mode.
JPL	28C256	32K x 8	CMOS/epi	SEQ	~3	5.0E-02			Jan-94			BNL	"Write" mode errors.
JPL	28C256	32K x 8	CMOS/epi	SEQ	7	2.0E-04			Jan-94			BNL	Perm. fail @ LET_{th}=60. Byte autoerasures in read mode @ LET ~4.
JH	28C256	32K x 8	CMOS	XIC					Apr-90	<<37		BNL	Kinnison
CNES	28C256	32K x 8	CMOS	XIC					1991	12	4.0E-03	IPN	R. Ecoffet et al, RADECS 91 Similar to Falquere. D/C 9032.

Heavy Ion SEE

Test Org.*	Device	Function	Technology	Mfr.	Effective SEU LET* Threshold	Device Xsection (cm^2)	Bits Tested	Bit Xsection (cm^2)	Test Date	LUth	LU Xsection (cm^2)	Fac.	Remarks 31-Aug-99
	Note: Entries in **RED** indicate data added since the 1997 Compendium.												
CNES	28C256	32K x 8	CMOS/epi	XIC					1992	12		IPN	Ecoffet. 1992; JH: 4/90. Stored data unaffected by LU. D/C 9032.
DASA/ESA	28C256-200	32K x 8	CMOS/epi (18µm) [SIG P402]	SEQ	3	1.5E-03			Nov-93	>74		BNL	Harboe-Sorensen. "Write errors only. "Read" is much less sensitive.
ARSP	28C256-250	32K x 8	CMOS/epi	SEQ	~3	1.0E-03			Mar-91			UCB	D/C 8946. Permanent error with Cu of 4.0E-04 cm^2.
ARSP	28C256-250	32K x 8	CMOS/epi	SEQ	10	2.0E-04			Mar-91			UCB	D/C 8946. Permanent error with Cu of 4.0E-04 cm^2.
GSFC	28C256A	32K x 8	CMOS, HMC's P512	SEQ/SEI	15 to 26				Jan-95	15 to 26		BNL	LaBel, et al. SEQ chip in SEI package. D/C 9224
GSFC	28C256E	32K x 8	CMOS/epi. SGN's Rev. J.	SEQ/SEI	7	5.0E-03		8.0E-08	Jan-95	>90		BNL	Permanent "write" failure LET = 60; 1.0E-05 cm^2. SGN D/C 9436
GSFC	28C256E	32K x 8	CMOS/epi. SGN's Rev. J.	SEQ/SEI	11			8.0E-08	Jan-95	>90		BNL	Permanent "write" failure LET = 60; 1.0E-05 cm^2. SGN D/C 9436
ESA	28C512D-15		CMOS	XIC	<~1.5	>3.0E-05	—		Jan-96			BNL	"Write" mode. Low LETs only. D/C 9144. Harboe-Sorensen, Ibid. above
LIN	28C64	8K x 8	CMOS/epi?	SEQ					1991	>164		BNL	Sferrino '91.
ESA	28C64C-20P1	8K x 8	CMOS	STM	<11				Jan-96	11 to 37	5.0E-06	BNL	Harboe-Sorensen, ESA Rept EWP-1859. "Read" mode. D/C 9248.
ESA	28C64C-20P1	8K x 8	CMOS	STM	>3				Jan-96	11 to 37	5.0E-06	BNL	Harboe-Sorensen, ESA Rept EWP-1859. "Write" mode. D/C 9248.
CNES	28HC256	32K x 8	HCMOS/ no epi	ATM	>54				1992			IPN	Falquere, RADECS 91, pg 479. Similar to CERTS data. D/C 9032.
ARSP	28HC256	32K x 8	HCMOS/ no epi	ATM	10	2.0E-03			Sep-89	>100		UCB	
CNES	28HC256	32K x 8	HCMOS bulk	SEQ	>54				1992	>120			Falquere, RADECS 91, pg 479. LU=?? D/C 9025. Like CERTS data.
ROCK	28HC64	8K x 8	HCMOS/ no epi	ATM	11	1.0E-04				>74		BNL	A. Waskiewicz. D/C 9148. Upsets captured are transients, not lost data.
ARSP	28HC64L	8K x 8	HCMOS/ no epi	ATM					Dec-89	>100		UCB	
ARSP	52B33	8K x 8	NMOS	SEQ	2	2.0E-04						UCB	Errors occur during Write/Erase only.
IBM	55C65	8K x 8	CMOS	SEQ	11	9.0E-04			Oct-92	>120		BNL	T. Scott
GSFC	**57C256F-35**		**CMOS**	**WSI**					**1997**	**<18.8**		**BNL**	**O'Bryan, et al, 98IEEE Wrkshp Rec., pg 39. D/C 9718.**
ESA	57C53B-5001	32K x 8	CMOS bulk (1.0 µm) P512	SEQ	~7	5.0E-05			1993	26	5.0E-05	BNL	Harboe-Sorensen, RADECS 93 preprint. D/C 9223B. LU in "read" mode.
GSFC	**AS58C1001SF-15E**	**128K x 8**	**CMOS**	**HTC**	**>37**				**1997**	**>37**		**BNL**	**O'Bryan, et al, 98IEEE Wrkshp Rec., pg 39. D/C 9646. Static mode testing.**
GSFC	**AS58C1001SF-15E**	**128K x 8**	**CMOS**	**HTC**	**~18.8**				**1997**	**>37**		**BNL**	**O'Bryan, et al, 98IEEE Wrkshp Rec., pg 39. D/C 9646. Programming mode testing. Block errors and one stuck bit @ LET ~37.**
JSC	CQ28C010	128K x 8	CMOS P512	SEQ					May-93	22	1.0E-04	BNL	Pat M. O'Neill. 400 mA LU currents. LU only
GSFC	**E28F016SB**	**1M x 16 Flash**	**CMOS**	**INT**	**9 to 11.4**					**26.2 - 29.9**	**1.0E-06**	**BNL**	**LaBel, et al, 96IEEE Wrkshp Rec., pg 19.**
JSC	FM1208S	512 x 8	TTL/CMOS	RMT	20	2.0E-04			May-93	25			Pat M. O'Neill (NASA-Johnson)
ESA	FM1208S	512 x 8	TTL/CMOS	RMT	20	2.0E-04			May-93	20	5.0E-05		Harboe-Sorensen, RADECS 93 preprint. D/C 9223B.
GSFC	HN58C1001	1M	CMOS/epi	HTC	18				Jan-95	>90		BNL	LaBel, et al, 96IEEE Wrkshp Rec., pg 19.

Test Org.*	Device	Function	Technology	Mfr.	Effective SEU LET* Threshold	Device Xsection (cm^2)	Bits Tested	Bit Xsection (cm^2)	Test Date	LUth	LU Xsection (cm^2)	Fac.	Remarks 31-Aug-99
	Note: Entries in **RED** indicate data added since the 1997 Compendium.												
GSFC	HN58C1001	1M	CMOS/epi	HTC	>80			5.0E-10	Jan-95	>90		BNL	LaBel, et al, 96IEEE Wrkshp Rec., pg 19.
JH	HN58C1001	1M	CMOS/epi	HTC	20	2.0E-05			Jun-95	>120		BNL	"Write"mode. Kinnison, memo 6/95. Compare earlier GSFC data.
JH	HN58C1001	1M	CMOS/epi	HTC	>120				Jun-95	>120		BNL	"Read" mode. Kinnison, memo 6/95. Compare earlier GSFC data.
ESA	HN58C256P-20	32K x 8	Die 58C256R	HTC	7	4.0E-04		2.0E-05		>120		BNL	"Write" errors. Harboe-Sorensen, RADECS 93 pg 490. D/C9232. Compare SEQ
ESA	HN58C66P-25	8K x 8	CMOS/epi	HTC	7 to 11	6.0E-04				>120		BNL	Harboe-Sorensen, 94IEEE TNS, No. 6, pg. 2340. Compared to flight data.
ESA	HN58C66P-25	8K x 8	CMOS/epi	HTC	53				1994	>84		BNL	Harboe-Sorensen, 94IEEE TNS, No. 6, pg. 2340. Compared to flight data.
JSC	KM29C010	32K x 8	CMOS	SAM	<<12	2.0E-02			May-93	>45		BNL	Pat M. O'Neill (NASA-Johnson)
JPL	M2864	8K x 8	NMOS	INT	<37	1.0E-04			Mar-86			UCB	Harboe-Sorensen, RADECS 93 pg 490. "Write" errors. D/C9232. Compare SEQ
ARSP	MD2815	2K x8	NMOS	INT	>120							UCB	No latchup.
MMS	MEM8129	128K x 8	Bulk CMOS with MNOS	HTC	4 to 10	1.0E-03						GANIL	Critical errors for worst case "write". Byte group errors.
ESA	MEM8129W-20	128K x 8	Hitachi 58C1000 die	HTC	12	2.0E-04			Jan-96	>53		BNL	Harboe-Sorensen, ESA/ESTEC Rept. No. EWP1859. D/C 9318.
GSFC	SA28C256ARP	32K x 8	CMOS	SPE	>15					15 to 26		BNL	LaBel, et al, 96IEEE Wrkshp Rec. pg. 19. LU obscures SEU.
GSFC	SA28C256ERPDB	32K x 8	CMOS/epi	SPE	7	1.0E-06			1995	>90		BNL	LaBel, et al, 96IEEE Wrkshp Rec. pg. 19. "Write" mode.
GSFC	SA28C256ERPDB	32K x 8	CMOS/epi	SPE	11	1.0E-06			1995	>90		BNL	LaBel, et al, 96IEEE Wrkshp Rec. pg. 19. "Read" mode.
GSFC	SA28C256ERPDB	32K x 8	CMOS/epi	SPE	>80					>90		BNL	LaBel, et al, 96IEEE Wrkshp Rec. pg. 19. "Static" mode.
SNL	SA3823		CMOS/SNOS (SNL design)	WEC	~35	1.0E-05			1994			BNL	Sexton, et al, 94IEEE Wrkshp Rec., pg 55.. Hard errors at LET=40 in write mode.
IBM	SMJ27C128-25	16K x 8	CMOS	TIX							1.0E-04		Pat M. O'Neill. 400 mA LU currents. LU only
JSC	WE-512K8-150CX	Four 128K x 8 dies	CMOS P512	SEQ					May-93	20	1.0E-04	BNL	P. O'Neil. Latchup-like response.
ARSP	X2816AM	2K x 8	NMOS	XIC	<54	3.0E-02						ORNL	
		UVEPROMs											
IBM	27C210	64K x 16	CMOS	INT	>6				Jan-93	45		BNL	LU_{th} not given; destructive at 0.9A. T. Scott, IBM letter
ARSP	27HC6642	8K x 8	CMOS	ATM	12	5.0E-05			Dec-89	15	7.0E-04	UCB	
ARSP	CY7C263	8K x 8	CMOS	CYP	10				Dec-89			UCB	
ESA	CY7C263-25PC	8K x 8	CMOS	CYP	<<26				Jan-96	<<26	2.0E-05	BNL	Harboe-Sorensen, ESA Rept EWP-1859. D/C 9224. Address errors.
ESA	D27C010-150V10	128K x 8	CMOS	INT	<<26*				Jan-96	<<26	1.0E-06	BNL	Harboe-Sorensen, ESA Rept EWP-1859. Die mark = 1988.
ESA	D27C2001D-15	256K x 8	CMOS	NEC	<<26*				Jan-96	<<26	2.0E-05	BNL	Harboe-Sorensen, ESA Rept EWP-1859. D/C 9150. *SEUs masked by LU.
ESA	HN27C101AG-15	128K x 8	CMOS	HTC	26 to 60				Jan-96	>82		BNL	Harboe-Sorensen, ESA Rept EWP-1859. D/C 9202. Transients.

Test Org.*	Device	Function	Technology	Mfr.	Effective SEU LET* Threshold	Device Xsection (cm^2)	Bits Tested	Bit Xsection (cm^2)	Test Date	LUth	LU Xsection (cm^2)	Fac.	Remarks 31-Aug-99
	Note: Entries in **RED** indicate data added since the 1997 Compendium.												
ESA	HN27C256HG-70	32K x 8	CMOS	HTC	<<26				Jan-96	60 to 82	6.0E-07	BNL	Harboe-Sorensen, ESA Rept EWP-1859. D/C 9212. Transients.
ESA	M27C1001-15FI	128K x 8	CMOS	SGS	<<26				Jan-96	>82		BNL	Harboe-Sorensen, ESA Rept EWP-1859. D/C 9227E5S. Transients.
ESA	M27C256B-15XFI	32K x 8	CMOS	SGS	<<26*				Jan-96	<<26	~1.0E-06	BNL	Harboe-Sorensen, ESA Rept EWP-1859. D/C 9222. *SEUs masked by LU.
ESA	M27C4001-12FI	512K x 8	CMOS	SGS	<<26				Jan-96	>82		BNL	Harboe-Sorensen, ESA Rept EWP-1859. D/C 9240B. Transients.
ESA	M27C512-15I	64K x 8	CMOS	SGS	<<26*				Jan-96	<<26	1.0E-05	BNL	Harboe-Sorensen, ESA Rept EWP-1859. D/C 9214. *SEUs masked by LU.
ESA	M5M27C101K-15	128K x 8	CMOS	MIT	<<26				Jan-96	>82		BNL	Harboe-Sorensen, ESA Rept EWP-1859. Transients.
ESA	M5M27C256K-12	32K x 8	CMOS	MIT	<<26				Jan-96	>82		BNL	Harboe-Sorensen, ESA Rept EWP-1859. Transients. (1/96)
ESA	SMJ27C040-12JM	512K x 8	CMOS	TIX	26 to 60**				Jan-96	>82		BNL	Harboe-Sorensen, ESA Rept EWP-1859. D/C IDL9226AI. **Transients.
ESA	SMJ27C512-20JM	64K x 8	CMOS	TIX	<<26				Jan-96	>82		BNL	Harboe-Sorensen, ESA Rept EWP-1859. D/C 9224A. Transients.
ESA	TC57256AD-12	32K x 8	CMOS	TOS	<<26				Jan-96	>82		BNL	Harboe-Sorensen, ESA Rept EWP-1859. D/C 9202EBI. Transients.
ESA	TC574000D-150	512K x 8	CMOS	TOS	60 to 82**				Jan-96	>82		BNL	Harboe-Sorensen, ESA Rept EWP-1859. D/C 9042EAK. **Transients.
ESA	TMS27C010A-15	128K x 8	CMOS	TIX	<<26*				Jan-96	<<26	4.0E-06	BNL	Harboe-Sorensen, ESA Rept EWP-1859. D/C 9222. *SEUs masked by LU.
JPL/ARSP	TMS27C256	32K x 8	HVCMOS epi/guard rings	TIX					1990	>120		UCB	Tested up to 60 deg C.
MMS	WSF57C49B	32K x 8	CMOS	WAF	45 (?)	5.0E-02			1992	<32	3.0E-04	GANIL	Dufour, et al, 92IEEE Wrkshp Rec., pg 21.
		Microprocessor (4-bit)											
JPL/ARSP	2901		CMOS with R=80 Kohms	SNL	>100		64						
JPL/ARSP	2901		CMOS with no register	SNL	>100		64						
JPL	2901A		Bipolar- LSTTL	AMD	~7	5.0E-03	64	7.8E-05					
JPL	2901-A1		Bipolar?	NSC	<3.3	1.0E-03	64	1.6E-05					27 MeV Carbon
JPL	2901-A2		Bipolar?	NSC	<3.3	1.0E-03	64	1.6E-05					27 MeV Carbon
JPL	2901-AX		Bipolar?	NSC	<3.3	1.0E-03	64	1.6E-05					27 MeV Carbon
JPL	2901B		Bipolar- LSTTL	AMD	~4	3.0E-03	64	4.7E-05					
ARSP	2901B		Bipolar- LSTTL	AMD	4	3.0E-04	64	4.7E-06					Test of RAM, Q-Reg., ALU & two latches.
JPL	2901C		Bipolar/ECL	AMD	<<3.3	3.0E-03	64	4.7E-05					
ARSP	2901C		Bipolar/ECL	AMD	<8	5.0E-04	64	7.8E-06					Test like AMD 2901B.
JPL	29F01		Bipolar-FAST	FAS	<6	3.0E-04	64	4.7E-06					26 MeV oxygen
ARSP	AMAS2901		CMOS/SOS	GPS	>120				1994			UCB	Koga

Test Org.*	Device	Function	Technology	Mfr.	Effective SEU LET* Threshold	Device Xsection (cm^2)	Bits Tested	Bit Xsection (cm^2)	Test Date	LUth	LU Xsection (cm^2)	Fac.	Remarks 31-Aug-99
	Note: Entries in **RED** indicate data added since the 1997 Compendium.												
ARSP	AMAS2901FB		CMOS	PLS	>120					>120		UCB	Koga
		Microprocessor (8-bit)											
JPL/ARSP	1802		CMOS	SNL	>120		256		Jun-93			UCB	
ARSP	6800		NMOS	MOT	7	3.0E-04	70	4.3E-06				UCB	
S^3	8085		NMOS	AMD	<6	3.0E-03	126	2.4E-05				UCB	Oxygen data to compare with INT 8085 data.
S^3	8085		NMOS	INT	<6	6.0E-05	126	4.8E-07				UCB	24 MeV O. Kr cross section predicted 1500 µm2 by analogy to AMD8085
JPL/ARSP	8085		NMOS	INT	<2.8	4.0E-03	126	3.2E-05	1987			UCB	Cross Section is for op register only.
JPL/ARSP	1802RH		CMOS	RCA	>120		256		Jun-83			UCB	
MHS?	80C31		CMOS/epi?	MHS							2.0E-05	GANIL	LU with ~3 GeV Kr. Menke's MHS letter is flawed DC9149
MHS?	80C31E (Temic type)		CMOS	MHS	5		50			>75			TEMIC/Matra MHS Radiation Evaluation Results Table July,1996
CNES	80C31L		CMOS/epi	MHS	~3	2.0E-03	1000	2.0E-06	Feb-89	>40		UCB	No LU >40. Aerospace at beam control. Compare previous entry
MHS?	80C32E (Temic type)		CMOS	MHS	5		40			>100			TEMIC/Matra MHS Radiation Evaluation Results Table July,1996
MHS	80C52µE		SCMOS1RT (epi, rad hard)	MHS								GANIL	T. Corbiere 4/94. No LU. Trans. power consumption probably induced by upset.
MHS?	80C52E (Temic type)		CMOS	MHS	5		40			>100			TEMIC/Matra MHS Radiation Evaluation Results Table July,1996
ARSP	80C85RH		CMOS/epi	HAR	35	1.0E-04	93	1.1E-06	Mar-87			UCB	5 V bias. No difference between this device and SNL SA3000.
ARSP	80C85RH		CMOS/epi	HAR	60		93					UCB	10 V bias. No difference between this device and SNL SA3000.
JPL	80C85RH		CMOS/epi	HAR	30	1.0E-04	93	1.1E-06	Jun-87	>120		UCB	5.5 V bias. No difference between this device and SNL SA3000. Also at BNL
JPL	80C85RH		CMOS/epi	HAR	>75		93		Jul-91			BNL	10 V bias. Little difference between older and newer HAR versions tested.
ARSP	8X300		Bipolar-TTL	SGN	18	2.0E-03	128	1.6E-05	Jun-93			UCB	Registers only.
ARSP	8X305		Bipolar-TTL	SGN	3	2.5E-03	128	2.0E-05	Jun-93			UCB	Registers only.
JPL	F9450		Bipolar-IIL	FAS	11				Oct-87			UCB	Nichols, et al, 88IEEE TNS, No. 6, pg 1619. High temp. data.
JPL	GP001	Slice	CMOS/SOS	RCA	>75		113						Old & new versions tested
CNES	MC80C52EH135-E		SCMOS1RT 1 µm (epi, rad hard)	MHS	~4	2.0E-03				>72		IPN	Estreme-Bezerra, CNES Rept. 6/94. D/C 9322.
ARSP	NSC800		CMOS	NSC	4		208			<20		UCB	
ARSP	SA3000		CMOS/epi	SNL	35	1.0E-04	93	1.1E-06	Mar-87			UCB	5 V bias. No difference between this device and HAR 80C85.
ARSP	SA3000		CMOS/epi	SNL	60		93					UCB	10 V bias. No difference between this device and HAR 80C85.
JPL	SA3000		CMOS/epi	SNL	30	1.0E-04	93	1.1E-06	Jun-87	>120		UCB	5.5 V bias. No difference between this device and HAR 80C85. Also at BNL

Test Org.*	Device	Function	Technology	Mfr.	Effective SEU LET* Threshold	Device Xsection (cm^2)	Bits Tested	Bit Xsection (cm^2)	Test Date	LUth	LU Xsection (cm^2)	Fac.	Remarks 31-Aug-99
	Note: Entries in **RED** indicate data added since the 1997 Compendium.												
JPL	SA3000		CMOS/epi	SNL	>75		93		Jul-91			BNL	
JPL	SBP9900		Bipolar-IIL	TIX	20	1.5E-04	346	4.3E-07				UCB	
ESA	Z80		NMOS	SGS	3	2.0E-03	208	9.6E-06				ESA	
ARSP	Z80		NMOS	ZIL	3	2.0E-04	208	9.6E-07	Nov-90			ORNL	Chapuis.
ARSP	Z84C00		CMOS	ZIL					Jun-88	25	2.5E-03	UCB	
		Microprocessor (16-bit)											
ESA	8086		NMOS/HMOS	INT	<3	1.0E-03	160	6.0E-06					
JH	80186		NMOS	INT	0.4	5.0E-04	~500			>100		BNL	R.Mauer (JH) estimate of tested bits.
JH	64500/1		CMOS/epi	LSI						75		BNL	1750A CPU
JPL/ARSP	80C 86		CMOS/bulk	HAR	<5	6.0E-02	~600	1.0E-04		11 to 18		UCB	
JPL/ARSP	80C 86		CMOS/epi	HAR	3	6.0E-02	~600	1.0E-04	Oct-87			UCB	Nichols, et al, 88IEEE TNS, No. 6, pg 1619. High temp. data.
ESA	80C 86		CMOS/epi	HAR	~1	2.4E-03	~600	3.0E-06	Oct-88			HARW	Harboe-Sorensen, ESTEC. Mask 1750.
ESA	80C 86		CMOS/epi	HAR	~1	2.4E-03	~600	4.0E-06	Oct-88			Cf-252	Harboe-Sorensen, ESTEC. Mask 1860. Compare facility below
ESA	80C 86		CMOS/epi	HAR	~1	2.4E-03	~600	2.0E-05	Jul-92			GANIL	Mask 1860. IEEE NS submittal--High energy ions. Compare facility above.
ESA	80C 86		CMOS/epi	HAR	~1	2.4E-03	~600	3.0E-05	Jul-91			GANIL	Mask 3584. IEEE NS submittal--High energy ions.
JPL/ESA/ SNL	80C 86		CMOS/epi	INT	1	4.0E-03	~600	6.5E-06	Oct-88			BNL	ESA: LET_{th}. JPL: LU w/heavy ions. SNL: LU w/(Cf-252 & protons)
ESA	80C 86		---	NEC	>>2.0				Oct-88			GANIL	See below. 171 MeV 0xygen only.
ESA	80C 86		---	OKI	>>3.1				Oct-88			GANIL	100 MeV Oxygen only.
ESA	80C 86-2/B		CMOS/epi	INT	~1			1.0E-05	Jul-92			GANIL	Harboe-Sorensen, 94IEEE TNS, No. 6, pg 2340.
JPL/JH	80C 86RH		CMOS/epi	HAR	3	1.7E-03			Apr-90	>75		UCB	JPL 2/89. Mask No. 3227: JH 4/90. D/C 8817. Rad-hard 80C86 version
JPL	80C 86RRH		CMOS/epi	HAR	3	8.5E-04			Feb-89	>100		UCB	Mask 3582. RH with SEU-hardened elements (only ½ the elements were hardened).
ARSP	80C186		CHMOSIII	INT	~9	1.0E-03	~600	2.0E-06	Oct-91	>100		UCB	
JPL	80C186		CHMOSIII	INT	~9	1.0E-03	~600	4.5E-06	Sep-92	>100		BNL	
GE	80C186		CHMOSIII	INT	4		510	2.0E-07	Jun-92	>110		BNL	
ARSP	80C286		CMOS	HAR	12	1.0E-03			1994	>90		UCB	Koga Priv. comm. ~1994. Compare earlier CMOS/epi data
ARSP	BX1750A		CMOS/epi (3 & 5 µm)	ASI	20	5.0E-04			May-90			UCB	
ARSP	F9445		Bipolar-IIL	FAS	20	1.5E-04	~128	~1.2E-06				UCB	

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Test Org.*	Device	Function	Technology	Mfr.	Effective SEU LET* Threshold	Device Xsection (cm^2)	Bits Tested	Bit Xsection (cm^2)	Test Date	LUth	LU Xsection (cm^2)	Fac.	Remarks 31-Aug-99
	Note: Entries in **RED** indicate data added since the 1997 Compendium.												
CNES	ISMT225	Transputer (16-bit core)	CMOS	ISM	2			2.0E-05	1995	36	1.0E-04	IPN	Bezerra, RADECS 95, pg 340. Dyn = short appl; static = reg/R: also 500 µm2 for cache
JPL	MA31750		CMOS/SOS	MED	175				Jun-92	>175		BNL	GEC-Plessey
JPL	MAS281		CMOS/SOS	MED	180		~200		May-89	>180		UCB	1750 Compatible. 504 MeV Xe @ 70° angle, 60 °C
ARSP	**MG80C186-12/B**	**NOP**	**CMOS III**	**INT**	**10**	**3.0E-04**			**1997**	**>63**		**UCB**	**Crain, et al, 98IEEE Wrkshp Rec., pg 51. D/C 8951. Lockup errors begin @ LET ~10.**
ARSP	**MG80C186-12/B**	**ALU, Bus Unit**	**CMOS III**	**INT**	**10**	**2.0E-04**			**1997**	**>63**		**UCB**	**Crain, et al, 98IEEE Wrkshp Rec., pg 51. D/C 8951. Lockup errors begin @ LET ~10.**
ARSP	**MG80C186-12/B**	**General Register**	**CMOS III**	**INT**	**10**	**7.0E-04**			**1997**	**>63**		**UCB**	**Crain, et al, 98IEEE Wrkshp Rec., pg 51. D/C 8951. Lockup errors begin @ LET ~10.**
ARSP	**MG80C186-12/B**	**Segment Register**	**CMOS III**	**INT**	**10**	**5.0E-04**			**1997**	**>63**		**UCB**	**Crain, et al, 98IEEE Wrkshp Rec., pg 51. D/C 8951. Lockup errors begin @ LET ~10.**
ARSP	MG80C286		CMOS/epi (7 µm)	HAR	>3	4.0E-03		1.0E-05	May-90	>63		UCB	Koga. D/C 8936. Lockup errors. LET_{th} of registers & ALU vary
ARSP	**MG80C286-12/883**	**NOP, ALU**	**CMOS/epi**	**HAR**	**10**	**5.0E-04**			**1997**	**>63**		**UCB**	**Crain, et al, 98IEEE Wrkshp Rec., pg 51. D/C 8936. Lockup errors begin @ LET ~5.**
ARSP	**MG80C286-12/883**	**General Register**	**CMOS/epi**	**HAR**	**10**	**1.0E-03**			**1997**	**>63**		**UCB**	**Crain, et al, 98IEEE Wrkshp Rec., pg 51. D/C 8936. Lockup errors begin @ LET ~5.**
ARSP	**MG80C286-12/883**	**Segment Register**	**CMOS/epi**	**HAR**	**10**	**7.0E-03**			**1997**	**>63**		**UCB**	**Crain, et al, 98IEEE Wrkshp Rec., pg 51. D/C 8936. Lockup errors begin @ LET ~5.**
ARSP	**MG80C286-12/883**	**Bus Unit**	**CMOS/epi**	**HAR**	**7**	**5.0E-03**			**1997**	**>63**		**UCB**	**Crain, et al, 98IEEE Wrkshp Rec., pg 51. D/C 8936. Lockup errors begin @ LET ~5.**
JPL	NS32081	Floating Pt. Unit	NMOS	NSC	<3	6.0E-03	>256					UCB	Only the eight 32-bit registers were tested
JPL	NS32C016		CMOS/epi (20 µm)	NSC	~3	2.0E-02	>368		Dec-86	3		BNL	Also proton-induced LU, Harvard, 6/91
ARSP	P1750A		CMOS/epi	PFS					~1994	>100		UCB	Koga
ARSP	P1750A		CMOS/SOS	PFS					1994	10		UCB	Koga
JH	P1750A		CMOS/SOS (3 chips)	PFS	20	3.0E-04	3 chips	5.0E-08	Jul-92	>>80		BNL	J. Kinnison, 92IEEE Wrkshp Rec., pg 12.
CNES	P1750A		CMOS/epi (9 µm)	PFS	5	(Partial)						IPN	F9450 Compatible. LU and SEU have same cross section
CNES	P1750A		CMOS/epi (9 µm)	PFS					Feb-90	<11	7.0E-03	GANIL	D/C 8918. 1.25 µm technology. Also tested at IPN
CNES	P1750AE		CMOS/epi (9 µm)	PFS					Feb-90	>11			D/C 8936. 1.0 µm technology.
JH	P1750AE		CMOS/epi (9 µm)	PFS					1989	50		BNL	Kinnison. Static test. See below.
GD	P1750AE		CMOS/epi (9 µm)	PFS					Apr-90	7			Dynamic test. See above. E. C. Smith
CNES	PACE1650A		CMOS/epi	PFS					Aug-90		1.0E-02	IPN	Chapuis. Also tested at GANIL.
JH	RTX2000		CMOS/epi	HAR					1991	>120		BNL	Kinnison
JH	RTX2010RH		Std. Cell TSOS-4 process	HAR	150				Jul-92	>150		BNL	J. Kinnison, 92IEEE Wrkshp Rec., pg 12.
JPL	SA3300		CMOS/bulk Twin Well	SNL	30				Oct-88			BNL	Unhardened clone of NS32016.
SNL	SA3300		CMOS/bulk Twin Well (2 µm)	SNL	35				Dec-90			BNL	F. Sexton, 89IEEE TNS, No. 6, pg. 1861.

Test Org.*	Device	Function	Technology	Mfr.	Effective SEU LET* Threshold	Device Xsection (cm^2)	Bits Tested	Bit Xsection (cm^2)	Test Date	LUth	LU Xsection (cm^2)	Fac.	Remarks 31-Aug-99
	Note: Entries in **RED** indicate data added since the 1997 Compendium.												
SNL	SA3300		CMOS/bulk Twin Well (1.25 µm)	SNL	23				Dec-90			BNL	F. Sexton, 89IEEE TNS, No. 6, pg. 1861.
JPL/SNL	SA3300		Above; with 80 kohm R.	SNL	>120				Oct-88	>120		BNL	
JPL	SBP9989		Bipolar-IIL (5 µm prototype)	TIX	~3	1.0E-04	336	~3.0E-07				UCB	
JPL	SBP9989		Bipolar-IIL (2 µm prototype)	TIX	12							UCB	
MMS	SBP9989-D		Bipolar-IIL	TIX	8	1.0E-02			1992	>104		GANIL	Dufour, et al, 92IEEE Wrkshp Rec., pg 21.
		Microprocessor (32-bit)											
CNES	68020		CMOS/epi	MOT	<1.7	1.0E-02			Jul-91	>54		IPN	Velazco, et al, 92IEEE Wrkshp Rec., pg.16. Register test
CNES	68020		CMOS/bulk	MOT	<1.7	1.0E-02			Jul-91	8	1.0E-02	IPN	Velazco, et al, 92IEEE Wrkshp Rec., pg.16. Register test
JH	68020		CMOS	MOT					1989	<40		Cf-252	Kinnison. See later data by CNES
JH	68020		CMOS/epi (15 µm)	MOT						<40		Cf-252 BNL	
JH	68020		CMOS/epi (12 µm) 1.35 µm features.	MOT						>50		Cf-252 BNL	
LIN	68020		CMOS/epi	MOT					Apr-91	32		BNL	
JPL	80386		CMOS	AMD	>>2.5				Jul-91	<24			
ARSP	68HC811		CMOS	MOT	3	3.0E-03			1995	8	8.0E-03	UCB	Koga
CNES	68T020		CMOS-SOI-0.8 µm (HSOI4CB)	TMS	7	1.1E-03	697		1994	>72		IPN	Lestrat, et al, 94IEEE TNS, No. 6, pg 2240. X-section = 2.4E-03 @ LET = 72.
JPL	**6x86-PR166+GP**	**166 MHz Pentium**	**CMOS**	**CYR**	**1.7**	**1.0E-04**			**Dec-97**			**TAM**	**JPL internal report. Cross section at LET = 37.**
NRL	79R3081	RISC	CEMOS-5 (6,8,10,12 µm epi)	IDT						12 to > 60	4.0E-03	BNL	Lestrat, et al, 94IEEE TNS, No. 6, pg 2240. LU = 12; 2.4E-03 @ LET = 72.
MMS	7C601	SPARC	CMOS bulk (0.8 µm)	CYP					1993	10	1.8E-02	GANIL	Beaucour, 93IEEE Wrkshp Rec. pg. 20.
JPL	80386DX		CMOS/epi (CHMOS III)	INT			4000	6.0E-07	Jul-88	>40		UCB	EAX register only.
IBM	80386DX		CMOS/epi (CHMOS III)	INT	6			~1.0E-06	Apr-89		1.0E-05	Cf-252	BNL, proton & alpha SEU tests also negative
IBM	80386DX		CMOS/epi (CHMOS IV)	INT	6			~1.0E-06	Apr-89		1.0E-05	Cf-252	Same as above, except CHMOS IV latched up. Also proton upsets
JPL	80386DX		CMOS/epi (CHMOS IV)	INT	2.5 to 4.5		272	~1.0E-06	May-91	40		BNL	
JPL	80386DX		CMOS/epi (CHMOS III)	INT			~60		Jul-88	>40		UCB	EAX register only.
IBM	80386DX		CMOS/epi (CHMOS III)	INT	6		~100		Apr-89			Cf-252	BNL, proton & alpha SEU tests also negative.
IBM	80386DX		CHMOS IV	INT	6		~100				1.5E-05	BNL	Also proton upsets.
JPL	80386DX		CHMOS IV	INT	2.5 to 4.5		~100		May-91	40		BNL	R. Watson et al.
GSFC	80386DX-20B & -25		CHMOS IV	INT	3.4	1.0E-03			Apr-95	29	1.0E-04	BNL	Moran, et al, RADECS 95, pg 263. Nondestructive LU.

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Test Org.*	Device	Function	Technology	Mfr.	Effective SEU LET* Threshold	Device Xsection (cm^2)	Bits Tested	Bit Xsection (cm^2)	Test Date	LUth	LU Xsection (cm^2)	Fac.	Remarks 31-Aug-99
	Note: Entries in **RED** indicate data added since the 1997 Compendium.												
GSFC	80486DX2-66		CHMOS V (0.8 µm)	INT	~5	2.0E-04			1995	>90	5.0E+00	BNL	Moran, et al, RADECS 95, pg 263. X-section with cache disabled. MicroLU @ LET > 20; < 1.0E-04 cm^2. Proton data also exists.
SEI	**80486DX2RP**	**50 MHz test frequency**	**CHMOS V (0.8 µm)**	**INT**	**<5.4**	**2.0E-03**			**1997**	**>40**		**BNL**	**Layton, et al, 98IEEE Wrkshp Rec., pg 170. D/C 9527527C. Cache on.**
SEI	**80486DX2RP**	**50 MHz test frequency**	**CHMOS V (0.8 µm)**	**INT**	**<5.4**	**1.5E-04**			**1997**	**>40**		**BNL**	**Layton, et al, 98IEEE Wrkshp Rec., pg 170. D/C 9527527C. Cache off.**
GSFC	80486DX-33		CHMOS IV (1.0 µm)	INT	~3	2.0E-04			1995	20		BNL	Moran, et al, RADECS 95, pg 263. X-section w/cache enabled. LU is catastrophic.
GSFC	80486DX-33		CHMOS IV (1.0 µm)	INT	5	~5.0E-05			1995	20		BNL	Same as above, x-section for cache disabled. Proton data exists.
JSC	**80486DX4**		**3LM CMOS [3.45V] 0.5 µm. Feature size.**	**AMD**	**1.5**	**2.5E-03**			**1996**	**~5**		**TAM**	**Kouba & Choi, Test Report 12/30/96 & 97IEEE Wrkshp Rec., pg 48. Threshold/X-sect with cache enabled. X-sect unsat. @ LET = 25. 8 error modes seen.**
JSC	**80486DX4**		**3LM CMOS [3.45V] 0.5 µm. Feature size.**	**AMD**	**4.5**	**2.5E-03**			**1996**	**~5**		**TAM**	**Same as above except threshold/cross section is with cache disabled .**
JSC	80486DX4		BiCMOS [3.3V] 0.6 µm feature size	INT	3.5	3.0E-04				~40		TAM	Kouba & Choi, Test Report 12/30/96. Threshold/cross section with cache enabled. Eight error modes seen.
JSC	80486DX4		BiCMOS [3.3V] 0.6 µm feature size	INT	6.5	3.0E-05				~40		TAM	Same as above except threshold/cross section is for cache disabled .
HAC	80960MX		CMOS	INT					Mar-93	15	1.0E-03	UCB	Two LU modes: 30 & 100's of mA. Shoga
CNES	90C601 SPARC601	SPARC	CMOS/bulk	MHS	2	8.0E-03				<13	2.0E-03	IPN Cf. 252	Estreme et al, 93IEEE Wrkshp Rec., pg 13. Registers only.
GSFC	**H30466A-21**		**CHMOS IV**	**SEI**	**5 to 6**				**1995**	**35 to 37.5**		**BNL**	**LaBel, et al, 96IEEE Wrkshp Rec., pg 19. MicroLU only. Count error cleared by reset.**
GSFC	**H30466A-21**		**CHMOS IV**	**SEI**	**3.4 to 5**				**1995**	**35 to 37.5**		**BNL**	**LaBel, et al, 96IEEE Wrkshp Rec., pg 19. MicroLU only. Reset errors.**
GSFC	**H30466A-21**		**CHMOS IV**	**SEI**	**6 to 11.4**				**1995**	**35 to 37.5**		**BNL**	**LaBel, et al, 96IEEE Wrkshp Rec., pg 19. MicroLU only. Lockup cleared by reset.**
JPL	**K5-PR166ABX**	**166 MHz Pentium**	**CMOS (3.5 V)**	**AMD**	**<0.4**	**6.3E-08**			**Jun-97**	**0.37**	**1.30E-06**	**BNL**	**Sat. LU x-section ~1.0E-01 cm^2. LU destructive.**
JPL	**K5-PR166ABX**	**166 MHz Pentium**	**CMOS (3.5 V)**	**AMD**	**<1.7**	**6.3E-08**			**Dec-97**	**1.7**	**~1.0E-06**	**BNL**	**Sat. LU x-section ~2.0E-03 cm^2. LU destructive.**
MMS	L64730	DCT processor	CMOS	LSI						8	2.0E-03	GANIL	Beaucour, et al, 93IEEE Wrkshp Rec. pg. 20.
JPL	L64801	Integer unit (SPARC)	"rad-hard" CMOS/epi (10 µm)	LSI	7	2.0E-05			Mar-94	15	8.0E-04	BNL	LU cross section @ LET = 60. See MMS data
MMS	L64811	SPARC	CMOS	LSI						8	5.0E-02	GANIL	Dufour, et al, 92IEEE Wrkshp Rec., pg 21..
CNES	L64811	SPARC	CMOS	LSI	2	2.0E-03			1993	~4	5.0E-02	IPN	Estreme et al, 93IEEE Wrkshp Rec., pg 13. Registers & applications
GSFC	**MG80486DX266**		**CHMOS IV**	**INT**	**~5**				**1997**	**~30**		**BNL**	**O'Bryan, et al, 98IEEE Wrkshp Rec., pg 39. D/C 9451. Dynamic tests with & without cache. Both data and lockup SEUs observed. Also microlatches and destructive SEL @ LET > 26.6.**
GSFC	Mongoose (R3000)	RISC	HCMOS/epi (1.0 µm)	LSI	23	4.0E-05			Apr-93	>85		BNL	LaBel, et al, 94IEEE Wrkshp Rec., pg 64. A RH version of R3000-based 'Cobra"
GSFC	**Mongoose V (R3000)**	**RISC**	**CMOS/SOI (Honeywell)**	**SYN**	**>83**				**1997**	**>96**		**BNL**	**O'Bryan, et al, 98IEEE Wrkshp Rec., pg 39. Cache off.**
GSFC	**Mongoose V (R3000)**	**RISC**	**CMOS/SOI (Honeywell)**	**SYN**	**~40**				**1997**	**>96**		**BNL**	**O'Bryan, et al, 98IEEE Wrkshp Rec., pg 39. Cache on**
GSFC	**MQ80386-25/B**		**CHMOS IV**	**INT**	**4 to 5**	**8.0E-05**				**30 to 32**		**BNL**	**LaBel, et al, 96IEEE Wrkshp Rec., pg 19. MicroLU only. Count or lockup cleared by reset.**
GSFC	**MQ80386-25/B**		**CHMOS IV**	**INT**	**5 to 6**	**1.5E-03**				**30 to 32**		**BNL**	**LaBel, et al, 96IEEE Wrkshp Rec., pg 19 . MicroLU only. Lockup cleared by reset.**

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Test Org.*	Device	Function	Technology	Mfr.	Effective SEU LET* Threshold	Device Xsection (cm^2)	Bits Tested	Bit Xsection (cm^2)	Test Date	LUth	LU Xsection (cm^2)	Fac.	Remarks 31-Aug-99
	Note: Entries in **RED** indicate data added since the 1997 Compendium.												
ALC	**PC603e**		**CMOS**	**MOT**	**~1.4**	**1.2E-02**	**65536**		**1997**	**>60**		**BNL IPN**	**Calvel, Static Data Cache Memory test (REGP603). Preliminary report**
CNES	**PC603e**		**CMOS**	**MOT**	**~1.5**		**5024**	**~1.5E-07**	**1998**	**>62**		**IPN PSI**	**Thomson Presentation. Static Data Cache Memory test (REGP603).**
ALC	**PC603e**		**CMOS**	**MOT**	**~1.7**	**1.0E-03**	**4096**		**1997**	**>60**		**BNL IPN**	**Calvel, Static Instruction Cache Memory test (REGI603). Preliminary report**
CNES	**PC603e**		**CMOS**	**MOT**	**~1.5**		**65536**	**~8.0E-09**	**1998**	**>62**		**IPN PSI**	**Thomson Presentation. Static Instruction Cache Memory test (REGI603).**
ALC	**PC603e**		**CMOS**	**MOT**	**~3.4**	**1.9E-03**	**65536**		**1997**	**>60**		**BNL IPN**	**Calvel, Static Register test (REGD603). Preliminary report**
CNES	**PC603e**		**CMOS**	**MOT**	**~1.5**		**65536**	**`3.0E-07**	**1998**	**>62**		**IPN PSI**	**Thomson Presentation. Static Register test (REGD603).**
LLNL	PR3400	RISC	CMOS PACE III (0.6 µm)	PFS	<3	1.0E-03				14 to 24	1.0E-04	UCB	J. Kimbrough, et al, 94IEEE TNS, No. 6, Pt II, p. 2706.
LLNL	PR3400A	RISC	CMOS PACE II (0.7 µm)	PFS	<3	1.0E-03				38 to 63	1.0E-05	UCB	J. Kimbrough, et al, 94IEEE TNS, No. 6, Pt II, p. 2706.
LLNL	PR3400L	RISC	CMOS PACE III (0.6 µm)	PFS	<3	1.0E-03				14 to 24	1.0E-04	UCB	J. Kimbrough, et al, 94IEEE TNS, No. 6, Pt II, p. 2706.
HAR	R3000	RISC	CMOS	IDT					May-91	4.8		BNL	VLSI MIPS RISC. D. Vail (HAR)
ESA	R3000	RISC	CEMOS IV	IDT			736		1992	<3.3		BNL	Harboe-Sorensen, et al, 92IEEE Wrkshp Rec., pg 34.
HAR	R3000	RISC	CMOS	LSI					May-91	53		BNL	VLSI MIPS RISC. D. Vail (HAR)
ESA	R3000	RISC	CMOS	LSI	~3		736	3.0E-06	1992	>60		BNL	Harboe-Sorensen, et al, 92IEEE Wrkshp Rec., pg 34.
ESA	R3000	RISC	CMOS	NEC	<10		736		1992	60		BNL	Harboe-Sorensen, et al, 92IEEE Wrkshp Rec., pg 34.
HAR	R3000	RISC	Adv. CMOS	PFS	<3.4	1.0E-03	~1300		May-91	>120		BNL	VLSI MIPS RISC. D. Vail (HAR)
ESA	R3000	RISC	PACE I	PFS	~6		736	1.0E-06	1992	>60		BNL	Harboe-Sorensen, et al, 92IEEE Wrkshp Rec., pg 34.
HAR	R3000	RISC	Adv. CMOS	SIE	6	1.0E-03	~1300		May-91	>120		BNL	VLSI MIPS RISC. D. Vail (HAR)
ESA	R3000	RISC	Adv. CMOS	SIE	<10		736	1.0E-06	1992	>60		BNL	Harboe-Sorensen, et al, 92IEEE Wrkshp Rec., pg 34.
HAR	R3000A	RISC	CMOS	IDT					May-91	26		BNL	VLSI MIPS RISC. D. Vail (HAR)
ESA	R3000A	RISC	CEMOS V	IDT	~6		736	>1.0E-06	1992	27		BNL	Harboe-Sorensen, et al, 92IEEE Wrkshp Rec., pg 34.
LLNL	R3000A	RISC	CMOS 6 (0.8 µm)	IDT	~5	1.0E-03				14 to 24	2.0E-04	UCB	J. Kimbrough, et al, 94IEEE TNS, No. 6, Pt II, p. 2706.
ESA	R3000A	RISC	HCMOS	LSI	<8		736	1.0E-06	1992	60		BNL	Harboe-Sorensen, et al, 92IEEE Wrkshp Rec., pg 34.
LLNL	R3000A	RISC	CMOS (0.7 µm)	LSI	<2.8	2.0E-03				38 to 63	2.0E-05	UCB	J. Kimbrough, et al, 94IEEE TNS, No. 6, Pt II, p. 2706.
LLNL	R3000A	RISC	CMOS	NEC	3	1.0E-03			Dec-94	38 to 63	6.0E-04	UCB	J. Kimbrough, et al, 94IEEE TNS, No. 6, Pt II, p. 2706.
HAR	R3000A	RISC	CMOS?	PFS					May-91	60		BNL	VLSI MIPS RISC. D. Vail (HAR)
ESA	R3000A	RISC	CMOS PACE II	PFS	<6		736	1.2E-06	1992	>60		BNL	Harboe-Sorensen, et al, 92IEEE Wrkshp Rec., pg 34.
LLNL	R3000A	RISC	CMOS PACE III (0.6 µm)	PFS	<3	2.0E-03			Dec-94	>63		UCB	J. Kimbrough, et al, 94IEEE TNS, No. 6, Pt II, p. 2706.

Test Org.*	Device	Function	Technology	Mfr.	Effective SEU LET* Threshold	Device Xsection (cm^2)	Bits Tested	Bit Xsection (cm^2)	Test Date	LUth	LU Xsection (cm^2)	Fac.	Remarks 31-Aug-99
	Note: Entries in **RED** indicate data added since the 1997 Compendium.												
ESA	R3000A	RISC	Adv. CMOS	SIE	~6		736	2.0E-06	1992	>60		BNL	Harboe-Sorensen, et al, 92IEEE Wrkshp Rec., pg 34.
LLNL	R3000A	RISC	CMOS	SIE	4	2.0E-03			Dec-94	>63		UCB	J. Kimbrough, et al, 94IEEE TNS, No. 6, Pt II, p. 2706.
LLNL	R33000HC	RISC	CMOS-- 1.0 µm.	LSI	3	5.0E-03			Dec-94	24 to 38		UCB	J. Kimbrough, et al, 94IEEE TNS, No. 6, Pt II, p. 2706.
IBM	RAD6000 FIxed Point		RHCMOS-E [CMOS/epi]	LFSC	15			1.2E-07	Jan-93	>120		BNL	Haddad. T > 120 deg C. FXPT chip (1 of 5 chips) simulates RH RSC6000.
HON	**RH-32**	**RISC**	**Honeywell HI Process**	**HON**	**~30**			**4.6E-07**	**1997**	**>83**		**BNL**	**Leavy, et al, 98IEEE Wrkshp Rec., pg 11.**
ESA	T414		CMOS/epi	ISM	3	2.0E-01	16K	2.0E-06				HARW	No latchup. Also tested with Cf-252.
ESA	T414		CMOS/bulk	ISM	3	2.0E-01	16K	2.0E-06				HARW	Latchup of on-chip RAM. Also tested with Cf-252.
MMS	T800	Transputer (32-bit)	CMOS	ISM						45	>1E-4	GANIL	
CNES	T805	Transputer (32-bit)	CMOS	ISM	~2			1.0E-05	1995	36		IPN	Bezerra, RADECS 95, pg 340. Register bit cross section (static). Dynamic = short applications; static = register
CNES	T805	Transputer (32-bit)	CMOS	ISM	~2			5.0E-06	1995	36		IPN	Bezerra, RADECS 95, pg 340 Cache bit cross section. Worst case is dynamic test with cache enabled.
ARSP	XC6802		CMOS	MOT					1994			UCB	Koga
ARSP	XC68302		CMOS	MOT	3	5.0E-04			1994	15	6.0E-03	UCB	Koga
		Microprocessor (64-bit)											
GDD	Alpha	MicroP (64-bit) RISC	CMOS	DEC					1993	<3.45	>5E-4		LaBel, et al, 93IEEE Wrkshp Rec., pg 27. X-section @ LET = 11.
		Microprocessor peripherals											
JPL	2909	4-bit Sequencer	Bipolar TTL	AMD	3	2.3E-04	46	5.0E-06					Stack plus Pointer
CNES	2910	4-bit ROM Sequencer	Bipolar TTL	AMD	3	4.0E-03	87	5.0E-05	Feb-89				Rept. by Chapuis-- with Aerospace.
ARSP	2914	4-bit Priority Interrupt Cntrlr	lBipolar TTL	AMD	5	5.0E-04	25	2.0E-05					
JPL	9407	4-bit Data Register	Bipolar TTL	FAS	<2.9	7.0E-04	32	2.2E-05				UCB	Four registers tested.
JPL	9407	4-bit Data Register	Bipola -IIL	FAS	15	1.4E-04	32	4.0E-06				UCB	Four registers tested. IIL appears to harder than TTL (above)
ARSP	82510	16-bit UART	CMOS	INT	~10			4.0E-05	1984			UCB	
JPL	2909 (SA3327)	4-bit Sequencer	CMOS with R=80 Kohms	SNL	>100		~26		1984			UCB	
JPL	2909 (SA3327)	4-bit Sequencer	CMOS with no resistor	SNL	50		~26		1984			UCB	
JPL	2909A	4-bit Sequencer	Bipolar TTL	AMD	<2.9	3.0E-04	46	>6.0E-06	1984			UCB	Stack plus Pointer
ARSP	2914Rev.	4-bit Priority Interrupt Cntrlr	Bipolar TTL	AMD	10	5.0E-04	25	2.0E-05					
JPL	81C55RH	Peripheral to 8085	CMOS/epi	HAR	40	4.0E-03	~2000	2.0E-06	Sep-91			UCB	RAM data at high LET.
GSFC	**82C54**	**Timer**	**CMOS**	**INT**	**9**				**1995**	**>80**		**BNL**	**LaBel, et al, 96IEEE Wrkshp Rec., pg 19.**

Test Org.*	Device	Function	Technology	Mfr.	Effective SEU LET* Threshold	Device Xsection (cm^2)	Bits Tested	Bit Xsection (cm^2)	Test Date	LUth	LU Xsection (cm^2)	Fac.	Remarks 31-Aug-99
	Note: Entries in **RED** indicate data added since the 1997 Compendium.												
IBM	ADS 10C00JT00	Disk Controller		WDC					May-93	>37		BNL	WP-02. Jim Pollack.
GSFC	**D8255A-5**	**Prog. Peripheral Interface**	**CMOS**	**INT**	**<3.6**				**1995**	**59.6**		**BNL**	**LaBel, et al, 96IEEE Wrkshp Rec., pg 19.**
MMS	**DP83932CVF**	**Network Interface Controller**	**M2CMOS (1 µm)**	**NSC**					**1995**	**15**	**3.0E-03**	**GANIL GSI**	**Poivey, et al, 96IEEE Wrkshp Rec., pg 73. D/C 9442**
MMS	**DP83950BVQB**	**Repeater Interface Controller**	**M2CMOS (1.5 µm)**	**NSC**					**1995**	**15**	**1.0E-03**	**GANIL GSI**	**Poivey, et al, 96IEEE Wrkshp Rec., pg 73. D/C 9506**
MMS	**DP83956AVLJ**	**Repeater Interface Controller**	**M2CMOS (1.5 µm)**	**NSC**					**1995**	**20**	**2.5E-03**	**GANIL GSI**	**Poivey, et al, 96IEEE Wrkshp Rec., pg 73. D/C 9452**
CNES	EF6821CM	Periph. Interface Adapter	NMOS	TMS	5	2.0E-03	48		Feb-89			UCB	Also tested at IPN with same results.
GSFC	HS2420	Sample & Hold Circuit	HCMOS rad hard (1.2 µm)	HAR	20	5.0E-06			Mar-93	>80		BNL	LaBel, et al, 94IEEE Wrkshp Rec., pg 64.
JPL	HS82C37ARH	16-bit DMA Cont. (80C86)	CMOS (junction isolation)	HAR	9	5.0E-04	~597		May-88	>50		BNL	Dynamic test mode. 244 bits tested.
JPL	HS82C54RH	16-bit Prog. Interval Timer	CMOS/epi (5 µm)	HAR	22		96		Feb-89	>80		UCB	Tested to T = 125 °C.
ESA	HS82C59A	16-bit Prority Interrupt Cont.	CMOS & CMOS/epi (12 µm)	HAR	20			4.0E-06	Jun-88			HARW	ESA: LU with Cf-252 in both bulk & 12 µm epi
ARSP	HS82C59A	16-bit Prority Interrupt Cont.	CMOS & CMOS/epi (12 µm)	HAR	16	2.0E-03			Feb-91			UCB	
JPL	HS82C85RH	16-bit Clock Generator	CMOS/epi (12 µm)	HAR	22		3/49		Feb-89	>80		UCB	No LU @ T = 70 deg C.
GSFC	IMSCO11	Data link- MicroP peripheral		ISM	~2	2.0E-04			1995	>72		IPN	Bezerra et al, RADECS 95, pg 340.
CNES	IMSCO11	Transputer link adapter		SGS	~2	2.0E-04				>72		IPN	Bezerra et al, RADECS 95, pg 340.
JPL	L29C520	Pipelined Register	CMOS	LDI					Mar-93	26	5.0E-05	BNL	
CNES	MD82C54	16-bit Prog. Interval Timer	CMOS/epi (12 µm)	HAR	10	4.0E-04	160		Feb-89	60		UCB	Non rad-hard part. T. Chapuis
GSFC	**M82C59A**	**Interrupt Controller**	**CMOS**	**HAR**	**11.4**				**1995**	**>80**		**BNL**	**LaBel, et al, 96IEEE Wrkshp Rec., pg 19.**
GSFC	**MQ82380-25/B**	**32-bit Integrated peripheral**	**CHMOS III**	**INT**	**3.4**				**1995**	**15 to 30**		**BNL**	**LaBel, et al, 96IEEE Wrkshp Rec., pg 19. Reset errors cleared by reset. MicroLU. Also a classic LU or SEE self-test?.**
JPL	NS32201	16-bit Timing Control Unit	Schottky Bipolar	NSC	~6	>3.0E-04	>2					UCB	Only Divide by 2 and Reset Flip-flops were tested.
ARSP	NSC810	4-bit I/O Port		NSC	18	3.0E-03	1000	3.0E-06		<40		UCB	Latchup <40
JPL	SA3304	16-bit Timing Control Unit	CMOS/bulk Twin Well	SNL	40				Nov-89			BNL UCB	Similar to NS32201. Current surges.
CNES	SOR 5053	Coder	CMOS	SOR					1990	9		IPN	Chapuis
GSFC	**TL7705**	**Power Supervisor**	**Bipolar TTL**	**TIX**	**3.38 - 4.5**	**8.0E-05**			**1996**	**>30**		**BNL**	**LaBel, et al, 97IEEE Wrkshp Rec., pg 14.**
GSFC	**TL7770-5**	**Power Supervisor**	**Bipolar TTL**	**TIX**	**7.5 - 11.6**	**1.0E-04**			**1996**	**>65**		**BNL**	**LaBel, et al, 97IEEE Wrkshp Rec., pg 14.**
IBM	WD33 92 A	SCSI Bus Controller		WDC	<<37				May-93	>37		BNL	Upset rates given. WP-02. Jim Pollack.
		Coprocessor (32-bit)											
CNES	68881	FPU	HCMOS/bulk	MOT						12			

Test Org.*	Device	Function	Technology	Mfr.	Effective SEU LET* Threshold	Device Xsection (cm^2)	Bits Tested	Bit Xsection (cm^2)	Test Date	LUth	LU Xsection (cm^2)	Fac.	Remarks 31-Aug-99
	Note: Entries in **RED** indicate data added since the 1997 Compendium.												
CNES	68882	FPU	CHMOS/epi	MOT	3	1.0E-02			Jul-91	<12			
CNES	68882	FPU	CMOS/bulk	MOT	3	1.0E-02			Jul-91	24 to 37			
CNES	68882	FPU	HCMOS/bulk	MOT						16.5			
GE	80387	Math Unit	CHMOS IV	INT	4				Oct-92	6			
JPL	80387	Math Unit	CHMOS IV	INT					Sep-91	24 to 37			
MMS	7C602	FPU	CMOS bulk (0.8 µm)	CYP					1993	10	2.0E-03		
MMS	7C604	MMU (SPARC)	CMOS bulk (0.8 µm)	CYP					1993	40			
GE	80387-16	Math Unit	CHMOS IV	INT					Oct-92	39 to 60			
GSFC	80387-20/B	Math Unit	CHMOS IV	INT	3.4	1.5E-04			May-95	27			
GSFC	80387-20/B	Coproc. (32-bit Math)	CHMOS IV (1.0 µm)	INT	3.4	1.5E–4				39 to 60	2.0E-05	BNL	Moran, et al, RADECS 95, pg 263.
GSFC	80387-20/B	Coproc. (32-bit Math)	CHMOS IV	INT	~10					~32		BNL	LaBel, et al, 96IEEE Wrkshp Rec., pg 19. MicroLU only?
CNES	90C602 SPARC602		CMOS/bulk	MHS	~4	2.0E-03			1993	8			
MMS	L64730	DCT processor	CMOS	LSI	8	2.0E-03			1992	8.7			
JPL	L64804	FPU (SPARC)	"rad-hard" CMOS	LSI	~4	1.5E-04			Mar-94	12			
CNES	L64814	FPU	CMOS	LSI	12	1.0E-01			1993	10			
MMS	L64814	FPU	CMOS/epi	LSI					1992	12			
CNES	MC68882	FPU	CMOS/epi E275(15 µm.)	MOT					Dec-90	>27			
GSFC	**MQ80387-20/B**	**Math Unit**	**CHMOS IV**	**INT**	**9 to 11.4**				**1995**	**32 to 35**		**BNL**	**LaBel, et al, 96IEEE Wrkshp Rec., pg 19. MicroLU.**
ESA	R3010A	FPU Accelerator	CEMOS V	IDT	<8	N/A			1992	27			
ESA	R3010A	FPU Accelerator	HCMOS	LSI	~8	N/A			1992	>27	6.0E-04		
ESA	R3010A	FPU Accelerator		PFS	<6	N/A			1992				
ESA	R3010A	FPU Accelerator	Adv. CMOS	SIE	~6	N/A			1992				
		Microcontroller											
JPL	68HCS705	8-bit	CMOS/epi	MOT					Jun-93	7	5.0E-03	BNL	Xsection @ LET=56; in standby mode. Part of RF modem.
BREL	87C51FB & 87C51FC	8-bit	CHMOSIII-E (256 byte RAM)	INT	~3		2300	4.0E-06	Aug-92	10	1.0E-03	UCB	Oberg, et al, 93IEEE Wrkshp Rec., pg 43. 256 byte RAM tested at 6V. See following. Proton upsets.
JPL	87C552 (inc. 80C51)	8-bit	CMOS	SGN					Jun-93	11	4.0E-03	BNL	Standard mode. MicroC has 80C51 microP
JPL	AM29CEPL154	MicroController	CMOS	AMD					Jun-92	10	2.0E-03	BNL	

Test Org.*	Device	Function	Technology	Mfr.	Effective SEU LET* Threshold	Device Xsection (cm^2)	Bits Tested	Bit Xsection (cm^2)	Test Date	LUth	LU Xsection (cm^2)	Fac.	Remarks 31-Aug-99
	Note: Entries in **RED** indicate data added since the 1997 Compendium.												
ARSP	AM85C30	8- or 16-bit Serial Communications Controller	CMOS	AMD					1994	20	1.0E-03	UCB	Koga
CNES	MHS80C31	8-bit	CMOS/epi (8 µm)	MHS					Oct-89	>37	4.0E-06	GANIL	D/C 8921
CNES	MHS80C31	8-bit	CMOS/epi (10 µm)	MHS					Feb-90	<25	2.0E-06	IPN	
BREL	RH80C51FC	8-bit	CMOS/epi	UTM	20	1.0E-04			1993	>37		UCB	Baze, et al, 93IEEE TNS, No. 6, pg 1703. Boeing redesign.
		Miscellaneous Controllers											
ESA	82380	DMA Controller (32-bit)	CHMOSIII, Jersusalem, mask B	INT	11		3552	1.0E-04	May-93	15	3.0E-06	BNL	Microlatchup. H. Van Looy, ESA Rept
ESA	53C90 MARS94 Flight	SCSI Controller	CMOS	NCR	>15				1993	15 to 26		BNL	Harboe-Sorensen, RADECS 93, pg 490. D/C 8923P. LU masked SEU X-section. Cf-252 failed to demonstrate LU.
ARSP	68HC811	Microcontroller(8-bit)	CMOS	MOT	3	3.0E-03				8	8.0E-03	UCB	Koga.
GSFC	82380-16 & -20/B	DMA Controller (32-bit)	CHMOSIII (1.5 µm)	INT	3.4	1.0E-04			May-95	12	1.0E-05	BNL	LaBel, et al, 92IEEE Wrkshp Rec., pg 1. Also Moran, et al, RADECS 95, pg 263
GSFC	82380-16 & -20/B	DMA Controller(32-bit)	CHMOSIII (1.5 µm)	INT	3.4	>1.0E-04				~12	~1.0E-05	BNL	LaBel, et al, 92IEEE Wrkshp Rec., pg 1. Also Moran, et al, RADECS 95, pg 263
SNL	82C527	CAN Controller (8-bit)	CHMOSIII (10 µm epi)	INT	2	5.0E-04	120		1994	17	3.0E-04	BNL	Sexton, et al, 94IEEE Wrkshp Rec., pg 55. No temp dependence.
GD	DDC61553	1553 Bus Controller	Hybrid CMOS	DDC								Cf-252	Latchup. See UTM UT1553.
MMS	DP83932CVF	Network Interface Cont.	M2CMOS (1 µm).	NSC						<15	3.0E-03	GANIL GSI	Poivey et al, 96IEEE Wrkshp Rec., pg 73. D/C 9442. Proton data also.
MMS	DP83950BVQB	Repeater Interface Cont.	M2CMOS (1.5 µm).	NSC						20	2.0E-04	GANIL GSI	Poivey et al, 96IEEE Wrkshp Rec., pg 73. D/C 9506.
MMS	DP83956AVLJ	Repeater Interface Cont.	M2CMOS (1.5 µm).	NSC						20	2.0E-04	GANIL GSI	Poivey et al, 96IEEE Wrkshp Rec., pg 73. D/C 9452. Proton data also.
ARSP	HS82C52	Serial Controller Interface	CMOS	HAR					Dec-91	50	2.0E-05	UCB	
ARSP	HS82C59A	Priority Interrupt Contrlr	lCMOS	HAR					Dec-91	16	2.0E-05	UCB	
ARSP	HS82C88	Bus Controller	CMOS	HAR					Dec-91	55	4.0E-06	UCB	
MMS	MA805	1553 Bus Controller	CMOS	MED						36	6.0E-05	GANIL	Dufour, et al, 92IEEE Wrkshp Rec., pg 21.
ARSP	SH451	SCSI Controller	CMOS	CIR								UCB	Koga. Latchup test only.
MMS	ULA 5N104	ASIC (Bus)	Bipolar	FER	<5.5	2.0E-03				>88		GANIL	Dufour, et al, 92IEEE Wrkshp Rec., pg 21.
		Op-Amp											
ADI	AD8001	800 mHz feedback	Bipolar-XFCB process	ADI	>82				1994	>82			M. DeLaus, 94IEEE Wrkshp Rec., pg 104.
ARSP	C12014	Programmable	CMOS	HAR	3	1.0E-03			May-90				Spikes
GSFC	EL2243	Analog	Bipolar	ELN	5	1.0E-03			1994	>90			LaBel, et al, 94IEEE Wrkshp Rec., pg 64.
LMM	**HS-1135**	**Rad-har, high speed, low power, current feedback**	**Bipolar, UHF-1**	**HAR**	**18.0**	**2.9E-04**			**97-98**	**>84**		**BNL**	**Bogorad, et al, 99NSREC Poster Paper PD-1 Preprint. Cross section for all 50 nS transients > 0.2 V.**
LMM	**HS-22620RH**	**Dual, rad-hard, wideband, high input impedance**	**Bipolar**	**HAR**	**18.0**	**5.6E-04**			**97-98**	**>84**		**BNL**	**Bogorad, et al, 99NSREC Poster Paper PD-1 Preprint. Cross section for all 0.5 µS transients > 1.0 V.**

Heavy Ion SEE

Test Org.*	Device	Function	Technology	Mfr.	Effective SEU LET* Threshold	Device Xsection (cm^2)	Bits Tested	Bit Xsection (cm^2)	Test Date	LUth	LU Xsection (cm^2)	Fac.	Remarks 31-Aug-99
	Note: Entries in **RED** indicate data added since the 1997 Compendium.												
ARSP	HS3530RH	Single, Low power	rad hard	HAR					Dec-93				Koga et al, 93IEEE TNS, No. 6, pg.1838. D/C 8839.
CNES/ARSP	LM108	Single, low bias	Bipolar	MOT	~2				1994	>27			Ecoffet et al, 94IEEE Worskhop Rec., pg 72.
GSFC	LM108	Single, low bias	Bipolar	NSC	<26				1994				LaBel, et al, 94IEEE Wrkshp Rec., pg 64. TID degradation at <2.5 krad obscured SEE data.
ARSP	**LM108**	**Op Amp**	**Bipolar**	**NSC**	**2**	**~5.0E-03**			**1997**	**>60**		**UCB**	**Koga, et al, 97IEEE TNS, No. 6, pg. 2325. D/C 9533. No LET_{th} dependence on input voltage delta.**
MMC	**LM108**	**Op Amp**	**Bipolar**	**NSC**	**1**	**1.7E-04**			**1997**	**>84**		**BNL**	**Bogorad, et al, 99NSREC Poster Paper PD-1 Preprint. Cross section for all transients > 0.2 V.**
JPL	LM108A	Single, low bias	Bipolar	LTN	<<7	6.0E-04			Nov-95				Transients only. Wide FWHM variability at LET=44.
JPL	LM108A	Op Amp	Bipolar	LTN					Nov-95	<<7	6.0E-04	TAM	Wide amplitude variability at LET = 44
GSFC	LM108AH	Single, low bias	Bipolar	PMI	24	5.0E-04			Jun-94	~60			LaBel. D/C B9412AD.
GSFC	LM124	Quad, low power	Bipolar	NSC					Jun-94	>90			LaBel
GSFC	LM158	Dual, low power	Bipolar	NSC					Jul-94	>100			LaBel. D/C AA0432458?
LMM	**LM158**	**Dual, low power**	**Bipolar**	**NSC**	**2.5**	**1.2E-04**			**97-98**	**>84**		**BNL**	**Bogorad, et al, 99NSREC Poster Paper PD-1 Preprint. Cross section for all 10 µS transients > 0.2 V.**
LMM	**LM158**	**Dual, low power**	**Bipolar**	**NSC**	**7.9**	**7.2E-05**			**97-98**	**>84**		**BNL**	**Bogorad, et al, 99NSREC Poster Paper PD-1 Preprint. Cross section for all 10 µS transients > 1.0 V.**
LMM	**LM158**	**Dual, low power**	**Bipolar**	**NSC**	**26.5**	**2.3E-05**			**97-98**	**>84**		**BNL**	**Bogorad, et al, 99NSREC Poster Paper PD-1 Preprint. Cross section for all 10 µS transients > 4.0 V.**
CNES	LM218H	Hi-slew rate, wide bandwidth	Bipolar	NSC					1994	>27			Ecoffet et al, 94IEEE Worskhop Rec., pg 72.
ARSP	OP-05	Low drift	Bipolar	PMI					Dec-93				Koga et al, 93IEEE TNS, No. 6, pg 1838. D/C 9206
GSFC	OP-07AJ	Low drift	Bipolar	PMI	12	3.0E-04			Jun-94	>50			LaBel 6/94. D/C 9345.
ARSP	OP-15	Single, bipolar JFET	Bipolar	PMI					Dec-93				Koga et al, 93IEEE TNS, No. 6, pg 1838. D/C 9240. No LU.
LMM	**OP-270**	**Very low noise, precision amplifier**	**Bipolar**	**ADI**	**7.5**	**1.4E-03**			**97-98**	**>84**		**BNL**	**Bogorad, et al, 99NSREC Poster Paper PD-1 Preprint. Cross section for all 0.5 µS transients > 1.0 V.**
LMM	**OP-270**	**Very low noise, precision amplifier**	**Bipolar**	**ADI**	**83.9**	**9.0E-05**			**97-98**	**>84**		**BNL**	**Bogorad, et al, 99NSREC Poster Paper PD-1 Preprint. Cross section for all 0.5 µS transients > 1.0 V.**
LMM	**OP-27A**	**Low noise, precision**	**Bipolar**	**ADI**	**7.9**	**1.3E-04**			**97-98**	**>84**		**BNL**	**Bogorad, et al, 99NSREC Poster Paper PD-1 Preprint. Cross section for all 1.0 µS transients > 0.2 V. Damage at LET = 83.9.**
LMM	**OP-27A**	**Low noise, precision**	**Bipolar**	**ADI**	**7.9**	**4.6E-05**			**97-98**	**>84**		**BNL**	**Bogorad, et al, 99NSREC Poster Paper PD-1 Preprint. Cross section for all 1.0 µS transients > 1.0 V. Damage at LET = 83.9.**
LMM	**OP-27A**	**Low noise, precision**	**Bipolar**	**ADI**	**26.5**	**3.0E-06**			**97-98**	**>84**		**BNL**	**Bogorad, et al, 99NSREC Poster Paper PD-1 Preprint. Cross section for all 1.0 µS transients > 4.0 V. Damage at LET = 83.9.**
LMM	**OP-37**	**Low noise, precision, high speed, voltage feedback**	**Bipolar**	**ADI**	**5.0**	**1.3E-04**			**97-98**	**>84**		**BNL**	**Bogorad, et al, 99NSREC Poster Paper PD-1 Preprint. Cross section for all 1.0 µS transients > 0.2 V. Damage at LET = 52.7.**
LMM	**OP-37**	**Low noise, precision, high speed, voltage feedback**	**Bipolar**	**ADI**	**8.8**	**4.4E-05**			**97-98**	**>84**		**BNL**	**Bogorad, et al, 99NSREC Poster Paper PD-1 Preprint. Cross section for all 1.0 µS transients > 1.0 V. Damage at LET = 52.7.**
LMM	**OP-37**	**Low noise, precision, high speed, voltage feedback**	**Bipolar**	**ADI**	**36.8**	**3.0E-06**			**97-98**	**>84**		**BNL**	**Bogorad, et al, 99NSREC Poster Paper PD-1 Preprint. Cross section for all 1.0 µS transients > 4.0 V. Damage at LET = 52.7.**
GSFC	**OP-400**	**Quad, low power, low offset**		**PMI**	**20**				**1997**	**>80**		**BNL**	**Crain, et al, 98IEEE Wrkshp Rec., pg 39. D/C 9711. Transients only. Minimum delta-V = 0.25V.**

Test Org.*	Device	Function	Technology	Mfr.	Effective SEU LET* Threshold	Device Xsection (cm^2)	Bits Tested	Bit Xsection (cm^2)	Test Date	LUth	LU Xsection (cm^2)	Fac.	Remarks 31-Aug-99
	Note: Entries in **RED** indicate data added since the 1997 Compendium.												
ARSP	**OP-42**	**High Speed, fast settling, precision Op Amp**	**Bipolar**	**ADI**	**2**	**~2.0E-03**			**1997**	**>60**		**UCB**	**Koga, et al, 97IEEE TNS, No. 6, pg. 2325.. D/C 9630. No LETth dependence on input voltage delta.**
LMM	**OP-42**	**High Speed, fast settling, precision Op Amp**	**Bipolar**	**ADI**	**7.9**	**8.7E-03**			**97-98**	**>84**		**BNL**	**Bogorad, et al, 99NSREC Poster Paper PD-1 Preprint. Cross section for all 2.0 µS transients > 0.2 V.**
LMM	**OP-42**	**High Speed, fast settling, precision Op Amp**	**Bipolar**	**ADI**	**18.0**	**3.9E-05**			**97-98**	**>84**		**BNL**	**Bogorad, et al, 99NSREC Poster Paper PD-1 Preprint. Cross section for all 2.0 µS transients > 1.0 V.**
LMM	**OP-42**	**High Speed, fast settling, precision Op Amp**	**Bipolar**	**ADI**	**18.0**	**1.7E-05**			**97-98**	**>84**		**BNL**	**Bogorad, et al, 99NSREC Poster Paper PD-1 Preprint. Cross section for all 2.0 µS transients > 4.0 V.**
LMM	**OP-467**	**Quad low noise, high speed amplifier**	**Bipolar**	**ADI**	**8.0**	**9.7E-04**			**97-98**	**>84**		**BNL**	**Bogorad, et al, 99NSREC Poster Paper PD-1 Preprint. Cross section for all 0.5 µS transients > 1.0 V.**
LMM	**OP-467**	**Quad low noise, high speed amplifier**	**Bipolar**	**ADI**	**15.0**	**4.9E-05**			**97-98**	**>84**		**BNL**	**Bogorad, et al, 99NSREC Poster Paper PD-1 Preprint. Cross section for all 200 nS transients > 1.0 V.**
GSFC	OP-97	Single, Low power	Bipolar	PMI					Jul-94	>110			LaBel. DC: unknown.
GSFC	PA10	Power	Bipolar	APX					Jul-94	>100			LaBel. D/C VE1009321.
LMM	**PM108**	**Op Amp**	**Bipolar**	**PMI**		**1.2E-04**			**97-98**	**>84**		**BNL**	**Bogorad, et al, 99NSREC Poster Paper PD-1 Preprint. All 15 µS transients > 0.2 V.**
JPL	RH1056	Op Amp	rad hard bipolar & JFET input	LTN					Nov-95			BNL TAM	At LET_{th} = 2, transients: 4 to 8 V for ~15 µsec; 1E-3 cm^2 @ LET = 44.
JPL	RH1056	Op Amp	rad hard bipolar + JFET input	LTN	1.45 [transients]	1.0E-03			Aug-95	>60		BNL	At LET_{th} = 3, transient pulses are 1.5 to 2.5 V for 5 to 10 µsec.
JPL	RH1056	Hi-speed instrt. rad-hard	rad hard bipolar & JFET in	pLTN					1996				For LET_{th}=2, transients: 4 to 8 V for ~15 µsec; 1.0E-03 cm^2 @ LET = 44.
JPL	RH108A	Single, low bias, rad-hard	rad hard bipolar	LTN	<<7	6.0E-04			Nov-95				
JPL	RH108A	Op Amp	rad hard bipolar	LTN					Nov-95	<<7	6.0E-04	TAM	Cross section @ LET = 44.
GSFC	SMP11	Sample-and-Hold	Bipolar-Super Beta transistors	PMI					Jul-94	>38			LaBel. D/C 085. None were functional post test.
		Optoelectronics											
JPL	**6N140**	**Darlington Amplifier**	**700µm (GaAsP) sandwich**	**HPA**	**11**				**1997**			**BNL**	**Johnston, et al, 98IEEE TNS Vol. 45, No. 6, pg 2867.**
JPL	**HCPL5203**	**Hi-gain Amp.**	**700µm (GaAsP) sandwich**	**HPA**	**0.3**	**~3.8E-03**			**1997**			**BNL**	**Johnston, et al, 98IEEE TNS Vol. 45, No. 6, pg 2867. No saturation X-section @ LET = 40.**
JPL	**HCPL5631 (6N134)**	**Hi-gain Amp.**	**700µm (GaAsP) sandwich**	**HPA**	**0.3**	**~2.6E-03**			**1997**			**BNL**	**Johnston, et al, 98IEEE TNS Vol. 45, No. 6, pg 2867. No saturation X-section @ LET = 30.**
GSFC	**HCPL5631 (6N134)**	**Hi-Gain Amp.**	**700 µm (GaAsP) sandwicl**	**HPA**	**38.2**	**4.5E-08**			**1997**			**UCD**	**LaBel, et al, 97IEEE TNS, Vol. 44, No. 6, pg 1885. D/C9247 & 9707.**
GSFC	**HCPL6651**			**HPA**	**<0.03**				**1997**			**BNL**	**O'Bryan, et al, 98IEEE Wrkshp Rec., pg 39. SET @ LET <0.03**
CNES	HSSR-7110	Power MOSFET optocoupler.	AIGaAs LED; n-ch MOSFET	HPA	>100					>100		BNL	LaBel, et al, 96IEEE Wrkshp Rec., pg 19.
		Other Linears											
LMM	**3261**	**Frequency Synthesizer**		**QLG**	**10**	**2.0E-03**			**97-98**	**>84**		**BNL**	**Bogorad, et al, 99NSREC Poster Paper PD-1 Preprint. Permanent frequency change. CMD required to recover.**
JPL	**37-97**	**Autocorrelator**	**CMOS (3.3 V)**	**ORB?**	**3.5**	**1.8E-06**			**Sep-98**			**TAM**	**Cross section saturation = 3.0E-04 @ LET = 80.**

Heavy Ion SEE

Test Org.*	Device	Function	Technology	Mfr.	Effective SEU LET* Threshold	Device Xsection (cm^2)	Bits Tested	Bit Xsection (cm^2)	Test Date	LUth	LU Xsection (cm^2)	Fac.	Remarks 31-Aug-99
	Note: Entries in **RED** indicate data added since the 1997 Compendium.												
JPL	54HC4046	Phase Lock Loop	HCMOS/bulk (3.5 µm).	NSC					Apr-95	>120			
GSFC	**AD630**	**Balanced Modulator**	**Bipolar**	**ADI**	**3.38**				**1996**		**>65**	**BNL TAM**	**LaBel, et al, 97IEEE Wrkshp Rec., pg 14. Short (<20 µs) errors.**
GSFC	**AD630**	**Balanced Modulator**	**Bipolar**	**ADI**	**17 7.4**				**1996**		**>65**	**BNL TAM**	**LaBel, et al, 97IEEE Wrkshp Rec., pg 14. Medium (20 - 100 µs) errors.**
GSFC	**AD630**	**Balanced Modulator**	**Bipolar**	**ADI**	**7.4**				**1996**		**>65**	**TAM**	**LaBel, et al, 97IEEE Wrkshp Rec., pg 14. Long (>100 µs) errors.**
MMS	AD630	Balanced Modulator		ADI	<7.4				Mar-97				LaBel, EEE Links
GSFC	**AD652**	**Voltage-to-Frequency Convert.**	**Bipolar**	**ADI**	**7.4**	**3.0E-03**			**1996**		**>64.7**	**BNL**	**LaBel, et al, 97IEEE Wrkshp Rec., pg 14. Single-bit SEUs.**
GSFC	**AD652**	**Voltage-to-Frequency Convert.**	**Bipolar**	**ADI**	**7.4**	**6.0E-05**			**1996**		**>64.7**	**BNL**	**LaBel, et al, 97IEEE Wrkshp Rec., pg 14. Double-bit SEUs.**
GSFC	**AD652**	**Voltage-to-Frequency Convert.**	**Bipolar**	**ADI**	**7.4**	**1.0E-04**			**1996**		**>64.7**	**BNL**	**LaBel, et al, 97IEEE Wrkshp Rec., pg 14. Multiple-bit SEUs.**
MMS	AD652	Voltage-to-Frequency Convert.	Bipolar	ADI	~7.4				Mar-97	>15			LaBel, EEE Links
MMS	AD783	Sample & Hold Amplifier	ABCMOS	ADI					Aug-95	>120		BNL	Up to 125 °C. ABCMOS technology = merged bipolar and CMOS.
JPL	CD54HC4046	Phase Lock Loop	HCMOS/bulk (3.0 µm).	HAR					Apr-95	>120			JPL Internal Report
GSFC	EMXO	Precision Oscillator	Hybrid Circuit	BAL	>85				Jul-93	>85			LaBel, et al, 93IEEE Wrkshp Rec., pg 27.
GSFC	**FUGA 15**	**Image Driver**	**CMOS**	**CCT**					**1997**	**11.4 to 12**		**BNL**	**O'Bryan, et al, 98IEEE Wrkshp Rec., pg 39.**
JPL	IMP 50E10	EPAC	CMOS/epi(15-20 µm.)	IMP	11	>>5E-5			Aug-95	15	~1E-4	BNL	EPAC [Elec. Prog. Analog Circuit] is a configurable group of analog elements. SEU cross section obscured by LU.
GSFC	IMP 50E10	EPAC		IMP	<1.5					15 to 27		BNL	LaBel, et al, 96IEEE Wrkshp Rec., pg 19. See preceding entry.
LMM	**LM2315**	**1.2 GHz Frequency Synthesizer**	**BiCMOS**	**NSC**	**23**	**4.3E-05**			**97-98**	**>84**		**BNL**	**Bogorad, et al, 99NSREC Poster Paper PD-1 Preprint. Permanent frequency change. CMD required to recover.**
ARSP	LTC1064	Low Pass Filter	CMOS	LTN					Dec-92	15	3.0E-04		W. Will (WP-01).
BREL	LTC1064	Low Pass Filter	CMOS	LTN					May-93	11	1.0E-02		W. Will (WP-01).
BREL	MC145158P2	PLL Freq. Synthesizer	Unknown. See DC's.	MOT	17+/-3	3.0E-04			May-93	>38			W. Will (WP-01). D/Cs QY9141 and QQST9217.
LMM	**PE3282A**	**1.1.GHzFrequency Synthesizer**	**UTSi(r)CMOS**	**PRG**	**34**	**5.0E-07**			**97-98**	**>84**		**BNL**	**Bogorad, et al, 99NSREC Poster Paper PD-1 Preprint. Permanent frequency change. CMD required to recover.**
HAC	Q3216	PWM	BiCMOS [no CMOS devices]	QAL	1	2.0E-03			1996	>62		UCB	Jobe, et al, 96IEEE TNS, No. 6, pg 2868. Serial & Parallel modes approx. same.
HAC	Q3236	PWM	BiCMOS [with CMOS devices]	QAL	1	2.0E-03			1996	>62		UCB	Jobe, et al, 96IEEE TNS, No. 6, pg 2868. Serial & Parallel modes approx. same.
GSFC	**QS3384DM**	**Quickswitch**	**CMOS**	**QSI**					**1995**	**15 to 18**		**BNL**	**LaBel, et al, 96IEEE Wrkshp Rec., pg 19.**
GSFC	SE5521F	Signal conditioner	Bipolar	SGN					Jul-94	>100			LaBel. D/C 012BD19-9401RD. .
LMM	**SG1525**	**PWM**	**Bipolar**	**SLG**	**18**	**1.2E-05**			**97-98**	**>84**		**BNL**	**Bogorad, et al, 99NSREC Poster Paper PD-1 Preprint. No double, but missing pulses.**
JPL	SG1526	PWM	Bipolar (+1 JFET)	SLG	10	2.0E-03			Sep-91	>110			
ARSP	**SG1549**	**Current Sense Latch**	**Bipolar**	**SLG**	**5**	**~3.0E-04**			**1997**	**>60**		**UCB**	**Koga, et al, 97IEEE TNS, No. 6, pg. 2325.. D/C 9627**

Test Org.*	Device	Function	Technology	Mfr.	Effective SEU LET* Threshold	Device Xsection (cm^2)	Bits Tested	Bit Xsection (cm^2)	Test Date	LUth	LU Xsection (cm^2)	Fac.	Remarks 31-Aug-99
	Note: Entries in **RED** indicate data added since the 1997 Compendium.												
LMM	**SG1825**	**PWM**	**Bipolar**	**SLG**	**11**	**7.5E-06**			**97-98**	**>84**		**BNL**	**Bogorad, et al, 99NSREC Poster Paper PD-1 Preprint. X-section for all 2 µS transients > 4.0 V. Double and missing pulses.**
LMM	**SP8855**	**2.8 GHz Parallel Load Frequency Synthesizer**		**PLS**	**6**	**1.1E-05**			**97-98**	**>84**		**BNL**	**Bogorad, et al, 99NSREC Poster Paper PD-1 Preprint. Permanent frequency change. CMD required to recover.**
LMM	**SP8858**	**1.5 GHz Frequency Synthesizer**		**PLS**	**7**	**3.7E-03**			**97-98**	**>84**		**BNL**	**Bogorad, et al, 99NSREC Poster Paper PD-1 Preprint. Permanent frequency change. CMD required to recover.**
ARSP	SP8908	PLL Divide by eight	Bipolar-ECL HE process	GEC-PLS	3	1.0E-04			1994				Shoga, et al, 94IEEE TNS, No. 6, pg 2252. Sophisticated phase & amplitude measurements.
GSFC	SSP-21110-025	Solid State Power Controller	Hybrid [ASICs, power FETs)	DDC					Feb-94	>80			LaBel. No transients, SEB or SEGR @ LET = 80.
LMM	**UC1705**	**PWM**	**Bipolar**	**UTR**	**18**	**1.5E-05**			**97-98**	**>84**		**BNL**	**Bogorad, et al, 99NSREC Poster Paper PD-1 Preprint. Transient duration = ±2.5/150 nS.**
ARSP	UC1802	PWM [low-P current mode]	BiCMOS	UTR	~1	5.0E-05			Dec-96	>63		UCB	Penzin et al, 96IEEE TNS, No. 6, pg 2968. Several SEU modes.
LMM	**UC1803**	**PWM**	**Bipolar**	**UTR**	**18**	**1.6E-03**			**97-98**			**BNL**	**Bogorad, et al, 99NSREC Poster Paper PD-1 Preprint. Damage observed @ LET = 11.1. Double and missing pulses.**
ALC	UC1806	PWM [1846 equivalent]	BiCMOS	UTR						>119		BNL	DC/DC reset errors "Not acceptable for any space application."
LMM	**UC1825**	**PWM**	**Bipolar**	**UTR**	**11**	**4.1E-06**			**97-98**	**>84**		**BNL**	**Bogorad, et al, 99NSREC Poster Paper PD-1 Preprint. X-section for all 2 µS transients > 4.0 V. Double and missing pulses.**
ARSP	UC1825A	PWM [high frequency]	Bipolar	UTR	~1	1.0E-02			Dec-96	>63		UCB	Penzin et al, 96IEEE TNS, No. 6, pg 2968. Several SEU modes.
ARSP	UC1845A	PWM [current mode]	Bipolar	UTR	~1	2.0E-04			Dec-96	>63		UCB	Penzin et al, 96IEEE TNS, No. 6, pg 2968. Several SEU modes.
LMM	**UC1864**	**PWM**	**Bipolar**	**UTR**	**6.25**	**4.1E-04**			**97-98**	**>84**		**BNL**	**Bogorad, et al, 99NSREC Poster Paper PD-1 Preprint. Double and missing pulses.**
		Resolvers											
HON	AD2S80	Resolver Dig. Conv.	Mixed Bipolar/ digital	ADI	3.4				Feb-93	>37		BNL	D/C 9227
NRL	**AD2S80**	**Resolver Dig. Conv.**	**Mixed Bipolar/ digital**	**ADI**	**8.75**	**7.5E-05**			**1998**	**>63**		**UCB**	**Buchner, et al, 99IEEE TNS Preprint.**
JPL	HSRD1056	Resolver Dig. Conv.	Hybrid RH CMOS	NTL	<13	5.0E-05			Dec-91	>110		BNL	
NRL	**RDC-19220**	**Resolver Dig. Conv.**	**CMOS**	**DDC**	**1**	**~8.0E-05**			**1998**	**5 to 15**	**~1.0E-03**	**UCB**	**Buchner, et al, 99IEEE TNS Preprint.**
		SCRs											
JPL	D1777A	Power SCR	Discrete. BV = 400V	SSD	>60				Jul-93	>115		BNL	No SCR turn-on at LET = 115.
JPL	DON688	Power SCR	Discrete. BV = 400V	SSD	>60				Jul-93	>115		BNL	No SCR turn-on at LET = 115.
		Voltage Comparator											
ARSP	**AD9696**	**Ultrafast, 200ps prop. delay**	**Bipolar**	**ADI**	**6**	**2.0E-06 - 1.0E-05**			**1997**	**>60**		**UCB**	**Koga, et al, 97IEEE TNS, No. 6, pg. 2325. D/C 9605. No LET_{th} dependence on input voltage delta.**
LMM	**CMP01**		**Bipolar**	**ADI**	**11.1**	**3.8E-04**			**97-98**	**>84**		**BNL**	**Bogorad, et al, 99NSREC Poster Paper PD-1 Preprint. X-section for all 2 µS transients > 0.2 V.**
LMM	**CMP01**		**Bipolar**	**ADI**	**26.2**	**2.2E-04**			**97-98**	**>84**		**BNL**	**Bogorad, et al, 99NSREC Poster Paper PD-1 Preprint. X-section for all 2 µS transients > 1.0 V.**
LMM	**CMP01**		**Bipolar**	**ADI**	**30**	**5.3E-05**			**97-98**	**>84**		**BNL**	**Bogorad, et al, 99NSREC Poster Paper PD-1 Preprint. X-section for all 2 µS transients > 4.0 V.**
CNES	LM111	Single	Bipolar	MOT	~2				1994				Ecoffet et al, 94IEEE Wrkshp Rec., pg 72. Transients > 2.4 V

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Test Org.*	Device	Function	Technology	Mfr.	Effective SEU LET* Threshold	Device Xsection (cm^2)	Bits Tested	Bit Xsection (cm^2)	Test Date	LUth	LU Xsection (cm^2)	Fac.	Remarks 31-Aug-99
	Note: Entries in **RED** indicate data added since the 1997 Compendium.												
JPL	LM111	Single	Bipolar	NSC	<7	3.0E-04			Nov-95				LET(th) < 7. Transient "+ or - " swing to rail: 4.0E-01 µsec @ LET=44
JPL	LM111	Single	Bipolar	NSC	<<7				Dec-96			TAM	Nichols, et al, 96IEEE TNS, No. 6, pg 2960. Transients @ LET<< 7 swing to rail: 3.0E-04 cm2 for 0.4 µsec
JPL	**LM111**	**Single**	**Bipolar**	**NSC**	**<1.45**				**Apr-96**			**BNL**	**Transient test only.**
ARSP	**LM111**	**Single**	**Bipolar**	**NSC**	**3 to 40**	**3.0E-06 - 1.0E-04**			**1997**			**UCB**	**Koga, et al, 97IEEE TNS, No. 6, pg. 2325.. D/C 9619. Very strong LETth dependence on input voltage delta.**
ARSP	LM111H	Single	Bipolar	NSC	15				Nov-93				Koga et al, 93IEEE TNS, No. 6, pg 1838. D/C 9151.
GSFC	LM119	Dual	Bipolar	NSC					Jul-94				LaBel. D/C 8830.
ARSP	**LM119**	**Dual**	**Bipolar**	**NSC**	**~3**	**~1.5E-04**			**1997**			**UCB**	**Koga, et al, 97IEEE TNS, No. 6, pg. 2325. D/C 9535. No LET_{th} dependence on input voltage delta.**
GSFC	LM139	Quad	Bipolar	NSC	50	2.0E-05			Feb-94				LaBel. Permenent current decrease at LET = 82.
JPL	LM139	Quad	Bipolar	NSC					Aug-95				For LET_{th} = 2, 2.5 µsec rail-to-rail transients; 6.0E-04 cm^2
JPL	LM139	Quad	Bipolar	NSC					Dec-96			BNL TAM	Nichols, et al, 96IEEE TNS, No. 6, pg 2960. Transients @ LET = 2, rail-to-rail; 6.0E-04 cm2 for 2 to 3 µsec.
JPL	LM139	Quad	Bipolar	NSC	2	4.0E-04				>60		BNL	For transients only. FWHM is 8 to 25 V for 0.5 to1.5 µsec.
JPL	**LM139**	**Quad**	**Bipolar**	**NSC**	**see remarks**	**3.2E-11**			**Feb-96**			**IUCF**	**200 MeV prot. Transients only. +25 mV input diff.**
JPL	**LM139**	**Quad**	**Bipolar**	**NSC**	**see remarks**	**1.23E-10**			**Feb-96**			**IUCF**	**200 MeV prot. Transients only. -25 mV input diff.**
JPL	**LM139**	**Quad**	**Bipolar**	**NSC**	**1.7**				**Apr-96**			**BNL**	**Transient test only.**
GSFC	**LM139**	**Quad**	**Bipolar**	**NSC**	**<10**				**1997**	**>37**		**BNL**	**O'Bryan, et al, 98IEEE Wrkshp Rec., pg 39.**
ARSP	**LM139**	**Quad**	**Bipolar**	**NSC**	**3 to 40**	**1.0E-04 - 3.0E-04**			**1997**			**UCB**	**Koga, et al, 97IEEE TNS, No. 6, pg. 2325.. D/C 9318. Very strong LETth dependence on input voltage delta.**
LMM	**LM139**	**Quad**	**Bipolar**	**NSC**	**8**	**4.3E-04**			**97-98**	**>84**		**BNL**	**Bogorad, et al, 99NSREC Poster Paper PD-1 Preprint. X-section for all 5µs >0.2V delta V = 300mV**
LMM	**LM139**	**Quad**	**Bipolar**	**NSC**	**8**	**2.7E-04**			**97-98**	**>84**		**BNL**	**Bogorad, et al, 99NSREC Poster Paper PD-1 Preprint. X-section for all 5µs >1V, delta V = 300mV**
LMM	**LM139**	**Quad**	**Bipolar**	**NSC**	**8**	**2.5E-04**			**97-98**	**>84**		**BNL**	**Bogorad, et al, 99NSREC Poster Paper PD-1 Preprint. X-section for all 5µs >4V, delta V = 300mV**
LMM	**LM139**	**Quad**	**Bipolar**	**NSC**	**8**	**1.9E-04**			**97-98**	**>84**		**BNL**	**Bogorad, et al, 99NSREC Poster Paper PD-1 Preprint. X-section for all 5µs >0.2V, delta V = 2V**
LMM	**LM139**	**Quad**	**Bipolar**	**NSC**	**36**	**2.3E-05**			**97-98**	**>84**		**BNL**	**Bogorad, et al, 99NSREC Poster Paper PD-1 Preprint. X-section for all 5µs 1V, delta V = 2V**
JPL	LM139	Quad	Bipolar	PMI					Aug-95				For LET_{th} << 7, 0.3 - 4 µsec rail-to-rail transients; 7.0E-04 cm^2.
JPL	LM139	Quad	Bipolar	PMI					Dec-96			TAM	Nichols, et al, 96IEEE TNS, No. 6, pg 2960. Transients @ LET = 1.4, rail-to-rail; 7.0E-04 cm2 for <4 µsec.
JPL	**LM139**	**Quad**	**Bipolar**	**PMI**	**<1.45**				**Apr-96**			**BNL**	**Transient test only.**
GSFC	LM139A	Quad	Bipolar	NSC					Jun-94			BNL	LaBel. D/C 9412.
GSFC	LM193H	Dual	Bipolar	NSC					Jul-94			BNL	LaBel. D/C 29344A.
LMM	**LM193H**	**Dual**	**Bipolar**	**NSC**		**8.40E-03**			**97-98**	**>84**		**BNL**	**Bogorad, et al, 99NSREC Poster Paper PD-1 Preprint. X-section for all 2 µS transients > 0.2 V.**

Test Org.*	Device	Function	Technology	Mfr.	Effective SEU LET* Threshold	Device Xsection (cm^2)	Bits Tested	Bit Xsection (cm^2)	Test Date	LUth	LU Xsection (cm^2)	Fac.	Remarks 31-Aug-99
	Note: Entries in **RED** indicate data added since the 1997 Compendium.												
LMM	**LM193H**	**Dual**	**Bipolar**	**NSC**	**8**	**2.7E-04**			**97-98**	**>84**		**BNL**	**Bogorad, et al, 99NSREC Poster Paper PD-1 Preprint. X-section for all 2 µS transients > 1.0 V.**
LMM	**LM193H**	**Dual**	**Bipolar**	**NSC**	**8**	**2.5E-04**			**97-98**	**>84**		**BNL**	**Bogorad, et al, 99NSREC Poster Paper PD-1 Preprint. X-section for all 2 µS transients > 4.0 V.**
LMM	**LT1018**	**Dual**	**Bipolar**	**LTN**	**3**	**2.4E-04**			**97-98**	**>84**		**BNL**	**Bogorad, et al, 99NSREC Poster Paper PD-1 Preprint. X-section for all 15 µS transients > 0.2 V.**
LMM	**LT1018**	**Dual**	**Bipolar**	**LTN**	**8.8**	**1.5E-04**			**97-98**	**>84**		**BNL**	**Bogorad, et al, 99NSREC Poster Paper PD-1 Preprint. X-section for all 15 µS transients > 1.0 V.**
LMM	**LT1018**	**Dual**	**Bipolar**	**LTN**	**26.2**	**1.1E-04**			**97-98**	**>84**		**BNL**	**Bogorad, et al, 99NSREC Poster Paper PD-1 Preprint. X-section for all 15 µS transients > 4.0 V.**
		Voltage Reference											
GSFC	LM136AH	+2.5 V ref.	Bipolar	NSC					Jul-94			BNL	LaBel. D/C 9320.
GSFC	**LM136AH**	**+2.5 V ref.**	**Bipolar**	**NSC**	**3.38**				**1996**			**BNL**	**LaBel, et al, 97IEEE Wrkshp Rec., pg14. Short (<1 µs) errors.**
ARSP	**REF-02**	**+5 V ref.**	**Bipolar**	**ADI**	**3 to 6**	**1.0E-04 - 5.0E-04**			**1997**	**>60**		**UCB**	**Koga, et al, 97IEEE TNS, No. 6, pg. 2325.. D/C 9305. Weak LET_{th} dependence on input voltage delta.**
GSFC	REF-02-373J	+5 V ref.	Bipolar	PMI					Jul-94	>100		BNL	LaBel. D/C Q8573944.
LMM	**RH1021**	**Precision Reference**	**Bipolar**	**LTC**	**18**	**1.4E-04**			**97-98**	**>84**		**BNL**	**Bogorad, et al, 99NSREC Poster Paper PD-1 Preprint. X-section for all 20 µS transients > 0.2 V. Includes 0.1 µf capacitor, Vin = 15 V through 511 ohms.**
LMM	**RH1021**	**Precision Reference**	**Bipolar**	**LTC**	**18**	**5.6E-04**			**97-98**	**>84**		**BNL**	**Bogorad, et al, 99NSREC Poster Paper PD-1 Preprint. X-section for all 5 µS transients > 0.2 V. No output capacitor, Vin = 15 V through 511 ohms.**
LMM	**RH1021**	**Precision Reference**	**Bipolar**	**LTC**	**18**	**1.1E-04**			**97-98**	**>84**		**BNL**	**Bogorad, et al, 99NSREC Poster Paper PD-1 Preprint. X-section for all 5 µS transients > 1.0 V No output capacitor, Vin = 15 V through 511 ohms.**
		Voltage Regulator											
GSFC	LM117H	Adjustable, +1.2 V to +37 V	Bipolar	NSC					Jul-94			BNL	D/C C92. LaBel
GSFC	LM120H-12/883C	Fixed, -15 V	Bipolar	NSC					Jul-94	>110		BNL	LaBel. D/C H2C9327A.
GSFC	LP2951	Fixed, +5 V	---	NSC	<26				Nov-94			BNL	LaBel
LMM	**RH1009**	**2.5 V shunt regulator diode.**	**Bipolar**	**LTC**	**7.5**	**5.2E-04**			**97-98**	**>84**		**BNL**	**Bogorad, et al, 99NSREC Poster Paper Preprint. X-section for all 20 µS transients > 0.2 V. Includes 0.1 µf output capacitor.**
LMM	**RH1009**	**2.5 V shunt regulator diode.**	**Bipolar**	**LTC**	**7.5**	**1.3E-03**			**97-98**	**>84**		**BNL**	**Bogorad, et al, 99NSREC Poster Paper Preprint. X-section for all 1 µS transients > 0.2 V. No output capacitor.**
LMM	**RH1009**	**2.5 V shunt regulator diode.**	**Bipolar**	**LTC**	**45**	**3.1E-05**			**97-98**	**>84**		**BNL**	**Bogorad, et al, 99NSREC Poster Paper Preprint. X-section for all 1 µS transients > 1.0 V. No output capacitor.**

Heavy Ion SEE

Test Org.*	Device	Function	Technology	Mfr.	Effective SEU LET* Threshold	Device Xsection (cm^2)	Bits Tested	Bit Xsection (cm^2)	Test Date	LUth	LU Xsection (cm^2)	Fac.	Remarks
													31-Aug-99
	Note: Entries in **RED** indicate data added since the 1997 Compendium.												
	*LET is effective (angle corrected) Linear Energy Transfer in MeV/(mg/cm2).												
Legend:													
	Manufacturers: ACT - ACTEL, Corp; ADA - Advanced Analog Devices; ADI - Analog Devices, Inc; AFX - Aeroflex Labs; AMD - Advanced Microdevices Corp; ASI - Allied Signal, Inc; ATT - American Telephone & Telegraph;												
	BAL - Ball Efatrom; BOE - Boeing Corp; BUB - Burr-Brown Corp; CCT - C-Cam Technology; CRY - Crystal Semiconductor; CYP - Cypress Corp; CYR - Cyrix; DAT - Datel; DDC - Data Device Corp; DEC Digital Electronic Corp;												
	FER - Ferranti; FOR - Force, Inc; GAZ - Gazelle Semiconductors; GIF - General Instruments, Corp; GTF - Gatefield; GIC - General Instruments Corp; HAM - Hamamatsu; HAR - Harris, Corp; HON - Honeywell; HPA - Hewlett-Packard;												
	HTC - Hitachi, Ltd; IBM - International Business Machines; IDT - Integrated Device Technology; IMP - IMP, Inc; INT - Intel Corp; ISM - Inmos, Corp; ISS - ISS, Inc; ITP - Interpoint; LMA - Lockheed-Martin; MAT - Matsushita, Corp;												
	MCN - Micron Technologies; MDI - Modular Devices, Inc; MED - Marconi Electonic Devices; MHS - Matra-Harris Semiconductor (France); MIC - Micrel Semiconductors; MIR - Micro-Rel Corp; MMI - Monolithic Memories;												
	MOT - Motorola Semiconductor Products; MPC - Micropac, Corp; MPS - Micro Power Systems; MXM - Maxim; NTL - Natel, Inc; NEC - Nippon Electric Corp; NCR - National Cash Register; NSC - National Semiconductor; OMR - Omnirel, Inc;												
	ONI - Optical Networks, Inc; OPT - Optek; ORB - Orbit Semiconductors; PFS - Performance Semiconductors; PHL - Phillips Laboratories; PLS - Plessey Semiconductor; PMI - Precision Monolithic, Inc; PRG - Peregrine; QLG - Qualcomm; QSI - Quickswitch, Inc; RAY - Raytheon;												
	RCA - Radio Corp of America; RMT - Ramtron; ROC - Rockwell International; SAM - Samsung; SCI - SCI Systems; SDL - Spectra Diode Labs; SIL - Siliconix; SGN - Signetics Corp; SNL - Sandia National Laboratories; SNY - Sony Corp; SYN - Synova;												
	SOR - Sorep (Europe); SPT - Signal Processing Technology; SRT - Saratoga Semiconductor; SSD - Solid State Devices; STC - Silicon Transistor Corp; TCS - Telecom Semiconductor; TEL - Teledyne Crystalonics; TIX - Texas Instruments;												
	TMS - Thompson-CSF; UTM - United Technologies Microelectronics Center; UTR - Unitrode; WEC - Westinghouse Electric; WSI - Western Semiconductor, Inc; XIC - Xicor, Inc; XIL - Xilinx Corp; YAM - Yamaha; ZOR - Zoran												
Test Organizations				**Radiation Facilities**									
	ALC - Alcatel Espace, France				BNL - Tandem Van de Graaff, Brookhaven National Laboratories, Long Island, NY								
	ARSP - Aerospace Corp., El Segundo, CA				Cf-252 - Cf-252 Fission Source (various facilities)								
	Ball Aerospace, Colorado Springs, CO				CYC - CYCLONE, Université Catholique de Louvain-la-Neuve, Belgium								
	BREL - Boeing Radiation Effects Laboratory, Seattle, WA				GANIL - GANIL Accelerator, France								
	CERT - CERT-ONERA, France				GSI - Gesellschaft fur Schwerionenforschung, Darmstadt, Germany								
	CLEM - Clemson University, Clemson, SC				HARW - Harwell Laboratory, Oxford, UK								
	CNES - Centre National d'etudes Spatiales, Toulouse, France				HCL - Harvard Cyclotron Laboratory, Boston, MA								
	DASA - Daimler Chrysler Aerospace, Munich, Germany				IPN - Insitute Physique Nuclaire, University of Orsey, France								
	ESA - European Space Agency, Noordwijk, Netherlands				IUCF - Indiana University Cyclotron Facility, Bloomington, IN								
	GD - General Dynamics, Azuza, CA				JAERI - Japanese Atomic Energy Research Institute, Japan								
	GE - General Electic, Valley Forge, PA				LLU - Loma Linda University Medical Center, Loma Linda, CA								
	GSFC - Goddard Space Flight Center, Greenbelt, MD				**NSCL - Michigan State University K1200 Superconducting Cyclotron, East Lansing, MI**								
	HAC - Hughes Aircraft Co, El Segundo, CA				ORNL - Oak Ridge National Labs, Oak Ridge, TN								
	HAR - Harris Corp, Melbourne, FL				PSI - Paul Scheerer Institute, Villigen, Switzerland								
	HON - Honeywell Space Systems, Clearwater, FL				SAT - SATURNE, CEA, Saclay, France								
	IBM - IBM Federal Systems Division, Manassas, VA				SPR - Sandia Pulse Reactor, Albuqueque, NM								
	ICI - Innovative Concepts Inc., McLean VA				TAM - Texas A&M University Cyclotron Institute K500 Superconducting Cyclotron, College Station, TX								
	JH - Johns Hopkins Applied Physics Lab, Laurel, MD				TIARA - Takasaki Ion Accelerators for Advanced Radiation Application, Japan								
	JPL - Jet Propulsion Laboratory, Pasadena, CA				TRI - TRI-University Meson Facility, Vancouver, British Columbia, Canada								
	JSC - Johnson Space Flight Center, Houston, TX				TSL - The Svedberg Laboratory, Uppsala, Sweden								
	LFS - Loral/Lockheed Federal Systems, Manassas, VA				TU - Tokyo University, Japan								
	LIN - MIT Lincoln Labs, Lexington, MA				UCB - 88-inch Cyclotron, University of California, Berkeley, CA								
	LIT - Litton, Huntsville, AL				UCD - University of California at Davis, Crocker Nuclear Laboratory, Davis, CA								
	LLNL - Livermore National Laboratories, Livermore, CA				UW - University of Washington cyclotron, Seattle, WA								
	LMC - Lockheed-Martin Corp, Sunnyvale, CA				VEC - Variable Energy Cyclotron, AERE, Harwell, UK								
	LMM - Lockheed Martin Missles and Space. Newtown, PA				WNR - Los Alamos National Laboratories, NM								
	LSI - LSI Logic, Milpitas CA				WU = Waseda Univ. (Japan).								
	McD - McDonald-Douglas, Newport Beach, CA												
	MHS - Matra Harris Semiconductor, France												
	MM - Martin Marietta Aerospace, Valley Forge, PA												
	MMS - Matra Marconi Space, France												
	MOT - Motorola Semiconductor Products, Phoenix, AZ												
	NASDA - National Space Development Agency of Japan, Tokyo, Japan												
	NRL - Naval Research Laboratory, Washington, DC												
	NSWC - Naval Surface Warfare Center, Crane, IN												
	ORNL - Oak Ridge National Labs, Oak Ridge, TN												
	ROCK - Rockwell Corp. (now Boeing), Anaheim, CA												
	SAAB - Ericsson Saab Avionics AB, Linköping, Sweden												
	SEI - Space Electronics, Inc, San Diego, CA												
	S^3 - S-Cubed, San Diego, CA												
	SNL - Sandia National Laboratories, Albuquerque, NM												

Test Org.*	Device	Function	Technology	Mfr.	Effective SEU LET* Threshold	Device Xsection (cm^2)	Bits Tested	Bit Xsection (cm^2)	Test Date	LUth	LU Xsection (cm^2)	Fac.	Remarks 31-Aug-99
	Note: Entries in **RED** indicate data added since the 1997 Compendium.												
Test Organizations (cont.)													
	SOR - Soreq NRC, Israel												
	UA - University of Arizona, Tuscon, AZ												
	US - University of Siegen, Germany												
	UTM - United Technologies Microelectronics Center, Colorada Springs, CO												
	UW - University of Washington, Seattle, WA												